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**SAFE
OPERATING
AREA**

- A switched-mode power supply with mains isolation for tv receivers
- Plumbicon camera tubes
- The safe operation of power transistors
- NORBIT 2 industrial control modules

Cover picture:

An understanding of SOAR curves is essential for all users of power transistors; a detailed article on the safe operation of such devices is contained in this issue.

A switched-mode power supply with mains isolation for tv receivers

A. P. A. van Beekvelt, F. A. van Heukelom, and G. Wolf

319

Product Information: Plumbicon camera tubes

343

The safe operation of power transistors

P. G. Noble

346

Product Information: NORBIT 2 industrial control modules

376

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Announcement

Mullard Technical Communications will shortly be replaced by a new journal, to be called Electronic Components and Applications. The start of 'ECA' is planned for August this year and all readers of MTC will automatically receive ECA through the same mailing list without needing to take any action.

As well as replacing Mullard Technical Communications, ECA will also be replacing a sister-journal called Electronic Applications Bulletin which is issued by Elcoma Publications, Philips, Eindhoven, The Netherlands.

The resources of both these existing journals will be pooled and so improvements are to be expected. The two writing and editorial teams will collaborate: material will be derived more freely from both sets of laboratories which have been previously accessed separately: up-to-date information about new electronic components will be derived from all parts of our organisation: every attempt will be made to keep the reader aware of developments in products and applications as they occur.

The journal itself will be noticeably different in character from its predecessors. A greater variety of information is planned, and the style of presentation will be changed where this is advantageous.

MTC will close with issue Number 140 at the end of Volume 14: this final issue will be dated October 1978 in the normal three-monthly sequence. We hope, however, to release issues Numbers 139 and 140 early, so that readers receive their last MTC before they receive their first ECA.

Mullard Technical Communications will have run for just over twenty-six years, since May 1952, and will have successfully carried news of our components and their applications to circuit designers throughout the world during all that time. In the new journal we are still addressing the same kind of reader, and we hope the new venture will be judged equally successful after a reasonable period. Every effort is being made to ensure that valid and useful information continues to flow.

We wish to repeat, and thereby emphasise, that readers need take no action to ensure that they continue to receive our journal. All readers will get the last MTC automatically and all readers will get ECA automatically. We hope that the change causes no confusion, and we hope that all our readers will come to share our view that, in this case at least, 'new' is 'better'.

Edmund G. Evans

Editor

A switched-mode power supply with mains isolation for tv receivers

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The last in a series of four articles about television switched-mode power supplies, this article describes a flyback converter circuit with mains isolation. The SMPS circuit is used also to provide direct drive to the horizontal deflection output transistor.

General principles of operation, and design considerations are given. A practical circuit for 220V mains is also included.

INTRODUCTION

This article is the last in a series of four (see Refs. 1, 2, and 3) about television switched-mode power supplies. In a previous article (Ref. 1) it was shown that, if mains isolation is required, the most convenient type of switched-mode power supply (SMPS) to use in a tv receiver is one which uses a flyback converter. It was also shown that it is advantageous to derive the drive for the horizontal deflection output transistor from the SMPS, and such a circuit is discussed in this article. The same design rules apply, however, to SMPS circuits in which the base drive facility is not used.

PRINCIPLES OF OPERATION

A simplified circuit diagram of an isolated flyback converter, together with associated waveforms and definitions, is given in Fig. 1. During the conduction period of the transistor (δT), energy is stored in the choke by an increasing current given by:

$$\Delta I_{L(\delta T)} = \frac{V_i}{L} \delta T. \quad \dots (1)$$

When the transistor ceases to conduct, the polarity of the voltage across the choke reverses and the stored

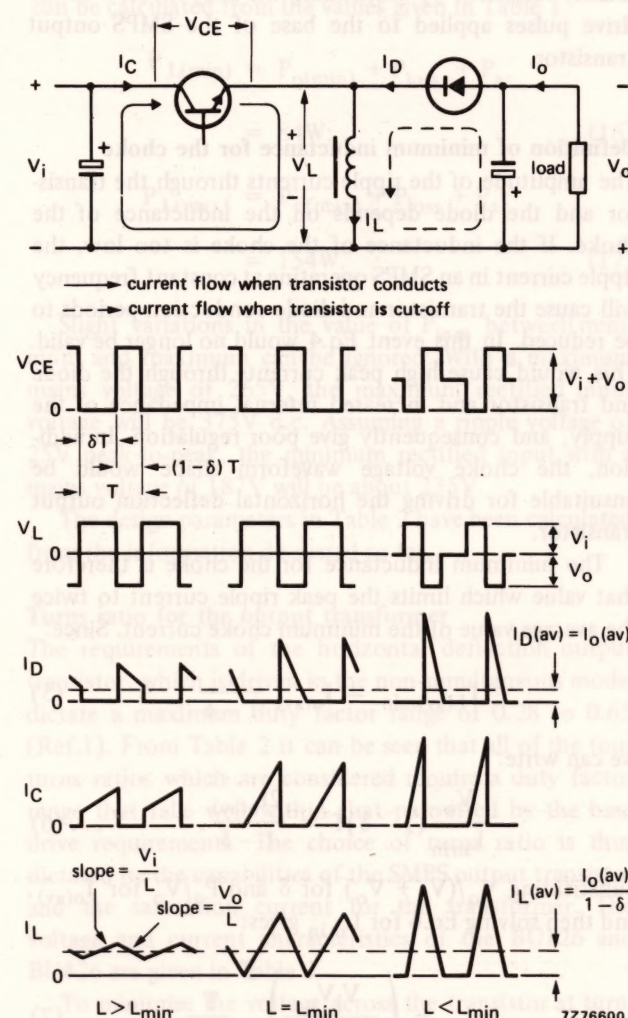


Fig. 1 — A flyback d.c.-to-d.c. converter circuit with waveforms showing the effect of variation of inductance of choke

energy is passed to the load via the flywheel diode. During this period $T(1-\delta)$, the decrease of current through the choke is given by:

$$T(1-\delta) = \frac{\Delta I_{L(1-\delta)} T}{V_o} = \frac{V_o}{L} T(1-\delta) \quad \dots (2)$$

Equilibrium is reached when the increase of choke current during the transistor conduction period is equal to the decrease of choke current during the period when the transistor is cut-off. This condition occurs when:

$$\frac{V_i}{L} \delta T = \frac{V_o}{L} T(1-\delta) \quad \dots (3)$$

Solving this equation for V_o gives:

$$V_o = V_i \frac{\delta}{1-\delta} \quad \dots (4)$$

The output voltage from this type of converter can therefore be stabilised against input voltage (rectified mains) variations by controlling the duty factor δ of the drive pulses applied to the base of the SMPS output transistor.

Definition of minimum inductance for the choke

The amplitude of the ripple currents through the transistor and the diode depends on the inductance of the choke. If the inductance of the choke is too low, the ripple current in an SMPS operating at constant frequency will cause the transistor and diode conduction periods to be reduced. In this event Eq.4 would no longer be valid. This would cause high peak currents through the diode and transistor and increased internal impedance of the supply, and consequently give poor regulation. In addition, the choke voltage waveform shape would be unsuitable for driving the horizontal deflection output transistor.

The minimum inductance for the choke is therefore that value which limits the peak ripple current to twice the average value of the minimum choke current. Since:

$$I_{L(av)min} = I_{o(av)} \frac{1}{1-\delta} \quad \dots (5)$$

we can write:

$$\frac{V_o}{L_{min}} (1-\delta) T = \frac{2I_{o(av)}}{1-\delta} \quad \dots (6)$$

Substituting $V_o/(V_i + V_o)$ for δ and P_o/V_o for $I_{o(av)}$, and then solving Eq.6 for L_{min} gives:

$$L_{min} = \left(\frac{V_i V_o}{V_i + V_o} \right)^2 \frac{T}{2P_o} \quad \dots (7)$$

Peak collector current for the SMPS output transistor

The SMPS output transistor peak collector current is:

$$I_{C(pk)} = I_{L(av)} + \frac{I_{ripple}}{2} \\ = \frac{I_{o(av)}}{1-\delta} + \frac{V_o T(1-\delta)}{2L} \quad \dots (8)$$

Substituting $V_o/(V_i + V_o)$ for δ , and P_o/V_o for $I_{o(av)}$ gives:

$$I_{C(pk)} = P_o \left(\frac{V_i + V_o}{V_i V_o} \right) + \frac{T}{2L} \left(\frac{V_i V_o}{V_i + V_o} \right) \quad \dots (9)$$

Isolation and auxiliary power

In a flyback converter, all of the energy transferred to the output capacitor has been previously stored in the

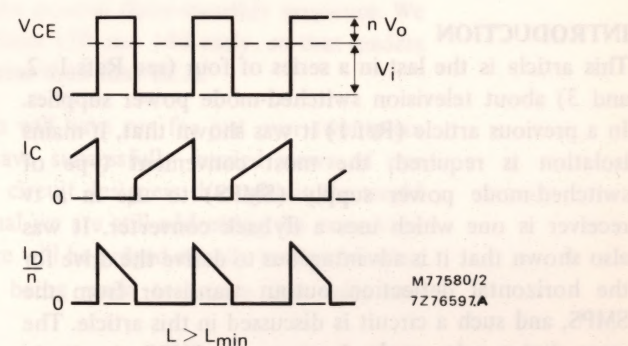
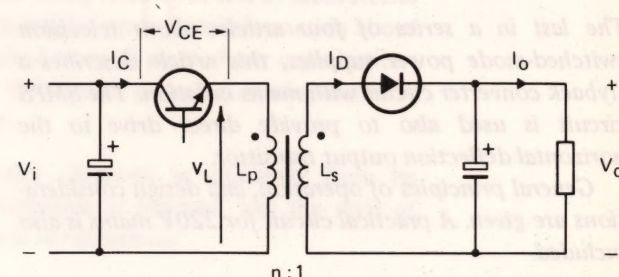


Fig.2 - A flyback d.c.-to-d.c. converter with isolation between input and output circuits

$$V_o = \frac{V_i}{n} \frac{\delta}{1-\delta} \\ L_{p(min)} = \left(\frac{V_i n V_o}{V_i + n V_o} \right)^2 \frac{T}{2P_o} \\ I_{C(pk)} = P_o \frac{V_i + n V_o}{V_i n V_o} + \frac{T}{2L_p} \frac{V_i n V_o}{V_i + n V_o} \\ V_{CE} = V_i + n V_o$$

choke. A secondary winding can therefore be added to the choke to achieve isolation between the input and output circuits. The main function of this component remains that of a choke; it will be referred to, however, as a transformer in the remainder of this article because of the use of such secondary windings. The turns ratio (n) of the primary and secondary windings has to be taken into account, and the flyback converter equations are modified with this factor as shown in Fig.2.

Auxiliary stabilised low voltages can be generated in the flyback converter by adding further secondary windings to the transformer. These voltages are then rectified by a diode that conducts during the same period as the flywheel diode. If the coupling between the secondary windings of the transformer is tight, the auxiliary load does not influence the current through the flywheel diode. The auxiliary load is therefore not limited by the requirement for a correct waveform at the main output. If auxiliary power is drawn from the supply, P_o is no longer used for the calculation of peak collector current and minimum transformer primary winding inductance. In this case P_o is replaced by P_L , the power that the switching transistor delivers to the transformer. P_L is given by:

$$P_L = P_o + P_a + P_{loss} \quad \dots (10)$$

where, P_o is the power delivered to the SMPS main (line) output, P_a is the power delivered to the SMPS auxiliary outputs, and P_{loss} is the power loss incurred between the switching transistor and the SMPS outputs.

DESIGN CONSIDERATIONS

The requirements in Table 1 relate to a specification for an SMPS for a colour tv receiver using the 20AX display system. Fig.3 is a simplified circuit of the output of such an SMPS. The driver and output stage of the vertical deflection circuit are supplied from the SMPS, but the power for the oscillator, ramp generator, and anti-bounce feedback circuit are derived from the scan voltage on the line output transformer. This arrangement ensures good tracking between line and field deflection. The class-B sound output stage, without shunt stabilisation, can be supplied from the SMPS when an additional CR filter is connected to the transformer secondary winding.

Initial design calculations

By inserting appropriate minimum and maximum values in the equations given in Fig.2, they can be rewritten:

$$L_{p(min)} = \left(\frac{V_{i(max)} n V_o}{V_{i(max)} + n V_o} \right)^2 \frac{T}{2P_{L(min)}} \quad \dots (11)$$

$$I_{C(pk)max} = P_{L(max)} \left(\frac{V_{i(min)} + n V_o}{V_{i(min)} n V_o} \right) + \frac{T}{2L_p} \left(\frac{V_{i(min)} n V_o}{V_{i(min)} + n V_o} \right) \quad \dots (12)$$

$$V_{CE(max)} = V_{i(max)} + n V_o \quad \dots (13)$$

The definitions of V_o given in Fig.2 can be expressed in terms of duty factor as follows:

$$\delta_{min} = \frac{n V_o}{V_{i(max)} + n V_o} \quad \dots (14)$$

$$\delta_{max} = \frac{n V_o}{V_{i(min)} + n V_o} \quad \dots (15)$$

The minimum and maximum values of P_L for the SMPS can be calculated from the values given in Table 1.

$$P_{L(min)} = P_{o(min)} + P_{loss} + P_a \\ = 84W \quad \dots (16)$$

$$P_{L(max)} = P_{o(max)} + P_{loss} + P_a \\ = 154W \quad \dots (17)$$

Slight variations in the value of P_{loss} between minimum and maximum can be ignored. With a maximum mains voltage of 265V, the maximum rectified input voltage will be 375V d.c. Assuming a ripple voltage of 25V peak-to-peak, the minimum rectified input with a mains voltage of 187V will be about 235V.

The design parameters in Table 2 have been calculated from the information discussed so far.

Turns ratio for the output transformer

The requirements of the horizontal deflection output transistor, which is driven in the non-simultaneous mode, dictate a maximum duty factor range of 0.28 to 0.65 (Ref.1). From Table 2 it can be seen that all of the four turns ratios which are considered require a duty factor range that falls well within that permitted by the base drive requirements. The choice of turns ratio is thus dictated by the capabilities of the SMPS output transistor and the saturation current for the transformer. The voltage and current characteristics of the BU126 and BU426 are given in Table 3.

To minimise the voltage across the transistor at turn-on, it is necessary for the SMPS output transformer to have a low turns ratio; on the other hand, a high turns

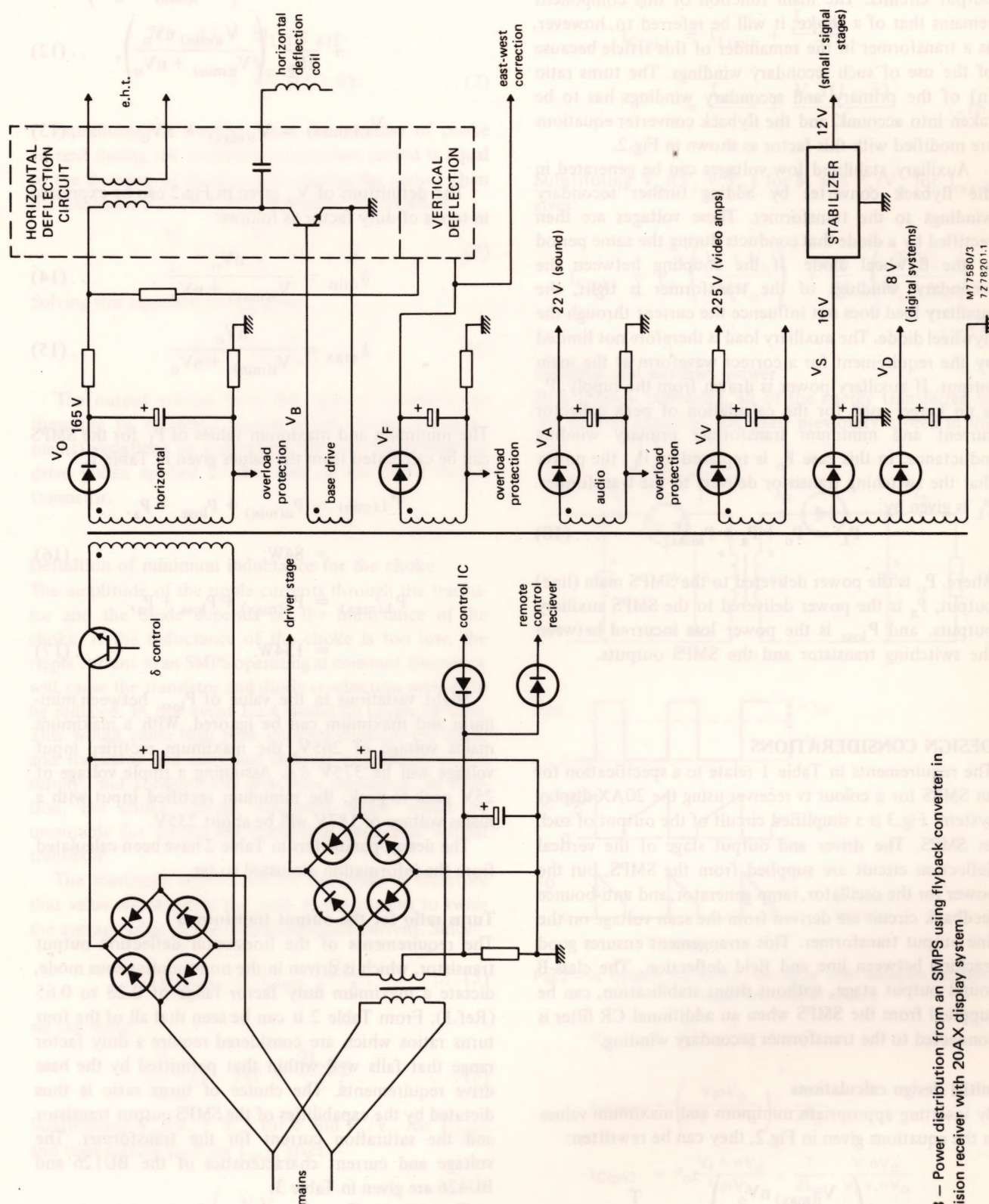


Fig. 3 — Power distribution from an SMPS using flyback converter in television receiver with 20AX display system

TABLE 1
Power Supply Requirements and Performance

SMPS outputs*	Output voltage (V)	Output power (W)		
		min	typ	max
Line	165 (V_o)	47		100 (P_o)
Field	35 (V_F)		15	(P_F)
Video	235 (V_V)	0		7 (P_V)
Audio	19 (V_A)	0		10 (P_A)
Small-signal	16 (V_S)		8	(P_S)
Base drive	4 (V_B)		4	(P_B)

Mains voltage range: $V_{\text{mains}} = 187$ to 264V a.c. Total auxiliary power: $P_a = P_F + P_V + P_A + P_S + P_B$ Losses in SMPS output circuit: $P_{\text{loss}} \approx 10\text{W}$

Stabilisation of line output: better than 3%

Ripple level: 50 and 100Hz mains hum, less than 0.2%

Switching frequency: $T = 64\mu\text{s}$, $f = 15\text{ 625Hz}$

*Although data for an 8V digital systems output is not given, there is provision for this

TABLE 2
Initial Design Calculations

Turns ratio (n)	1.0	1.2	1.5	1.8	
V _{CE(max)} (turn-on)	540	573	622	672	V
L _{p(min)}	5.0	6.4	8.5	10.5	mH
I _{C(max)}	2.2	2.0	1.7	1.6	A
δ _{min}	0.31	0.35	0.4	0.44	
δ _{max}	0.41	0.45	0.51	0.55	

TABLE 3
Characteristics of SMPS Output Transistor

	$V_{CE(\text{max})}$ (turn-on) (V)	V_{CESM} (V)	$I_{C(\text{max})}$ d.c. (A)	I_{CM} (A)
BU126	600	750	3	6
BU426	700	800	6	8

ratio minimises the output transistor collector current. The DT2098/01 transformer has a turns ratio of 1.2:1 which results in a maximum peak collector current of 2A and a maximum collector-emitter voltage of 573V. To obtain more SMPS output power without exceeding the value of $I_{C(pk)max}$ given in Table 3, the transformer turns ratio may be increased to 1.8:1. In this event transistor type BU426 should be used rather than type BU126.

Inductance and coupling factor for the output transformer

We have already arrived at a definition for the minimum choke inductance but no mention has yet been made of an upper limit. From the point of view of restricting the peak value of the transistor and diode currents, it would seem that a large inductance is desirable. There are, however, other conflicting factors to be taken into account. The energy in the inherent leakage inductance of the transformer is $L_{leak} I^2 / 2$.

This energy causes the waveform of the collector-emitter voltage of the transistor to exhibit an overshoot at turn-off. The overshoot must be suppressed by a damping network. Since such a network causes losses, the leakage inductance must be minimised by using a transformer with a low-inductance primary winding and tight coupling between windings. A low-inductance primary winding also helps in the design of a low-loss transformer. In the table of initial design calculations, it was shown that the minimum inductance for the primary winding of a transformer with a turns ratio of 1.2:1 is 6.4mH. The nominal inductance of the primary winding of the transformer type DT2098/01 is 7mH.

Core of the output transformer

The SMPS output transformer type DT2098/01 is wound on an E46 Ferroxcube core which, because of its large

cross-section, reduces the number of turns required. The broad winding window allows each winding to be constructed in a single layer. This arrangement also necessitates the use of only one pair of screens to reduce asymmetrical mains pollution. The creepage distance is in accordance with IEC mains-isolation recommendations contained in IEC publication No.65 (1967).

Output stage

The appendix to this article discusses typical precautions taken to ensure that the SMPS output transistor operates within its SOAR (safe operating area; see Refs.5 and 6). These safety precautions and the precautions that have to be taken to prevent SMPS-generated interference manifesting itself on the television screen have some factors in common. In the output circuit of the SMPS under discussion, two techniques shown in Fig.4 reduce radiated interference (see also Fig.20, later). Firstly, the output transistor is connected at the upper end of the transformer primary winding: this arrangement ensures that the stray capacitances at the collector of the transistor are maintained at a constant potential, thus preventing switching spikes. Secondly, capacitor C_1 in parallel with the primary winding of the transformer reduces the rate of change of voltage (dV/dt) at that point and minimises the length of the interference radiation loop.

Examination of the output circuit to determine whether there is any necessity of further transistor protection (to ensure operation within the SOAR) raises the following points.

- 1) The presence of C_1 eliminates the need of a 'slow-down network' as shown in parallel with the transistor in Fig.4.
- 2) The peak current through C_1 during transistor turn-on must be limited by connecting a small choke L in series with the transistor.

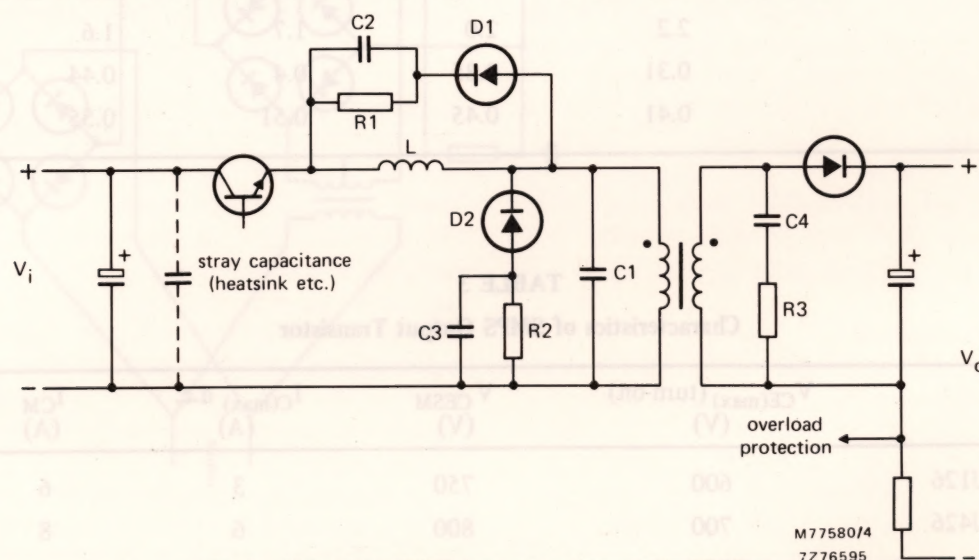


Fig.4 — Maintaining SMPS output transistor within SOAR

- 3) Network D_1/R_1 must be connected in parallel with the small choke. This network damps the LC_1 oscillations when the transistor is turned on, and absorbs the energy stored in L when the transistor is turned off: capacitor C_2 permits passage of the peak current, thereby minimising the peak voltage across the transistor.

- 4) An overshoot is caused by the transformer leakage inductance during the transistor turn-off period. To clip this overshoot, another network (D_2, R_2 , and C_3) must be connected in parallel with the primary winding of the transformer.

Although the protection of the transistor is now complete, a further network R_3, C_4 is incorporated to damp ringing at the secondary winding of the transformer and to limit the reverse voltage across the flywheel diode.

Driver stage

The SMPS output stage incorporates a high-voltage silicon npn transistor type BU426 which is specifically intended for use in television SMPS circuits. Turn-on losses in the output stage must be minimised by ensuring that the drive circuit provides a fast-rising base current. This current must maintain sufficient amplitude to ensure a low saturation voltage throughout the conduction period of the output transistor. Turn-off losses must also

be minimised by ensuring adequate duration of reverse base current after the collector current of the output transistor has started to decrease. Further requirements for the driver stage are:

- 1) the ability to operate satisfactorily within the duty factor range of the SMPS (including slow-start when the duty factor is small);
- 2) the ability to maintain the output transistor in the non-conducting state for long periods (following operation of protection circuits or remote switch-off);
- 3) the provision of adequate current gain between the control IC and the SMPS output transistor;
- 4) a short storage time to ensure that the drive-current duty factor dictated by the control circuit is faithfully reproduced.

A typical driver stage that fulfils the foregoing requirements is shown in Fig.5.

Output-transistor base circuit during turn-on

When the drive transistor ceases to conduct, forward base current is delivered to the output transistor by virtue of the energy stored in the core of the transformer. To ensure a short rise-time for the base current, R_2 and C_2 (which limit the ringing on the collector voltage waveform of the drive transistor) under-damp the transformer. This arrangement provides a degree of overshoot

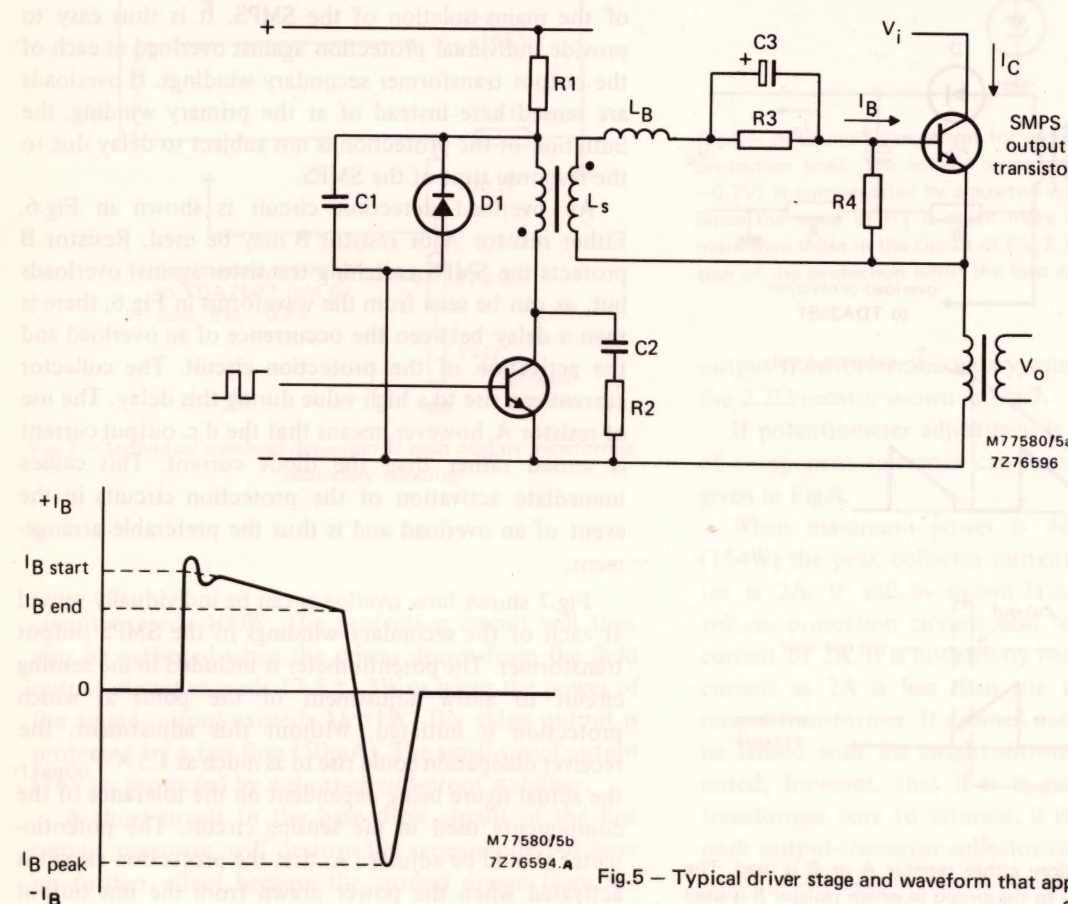


Fig.5 — Typical driver stage and waveform that appears at the base of the SMPS output transistor

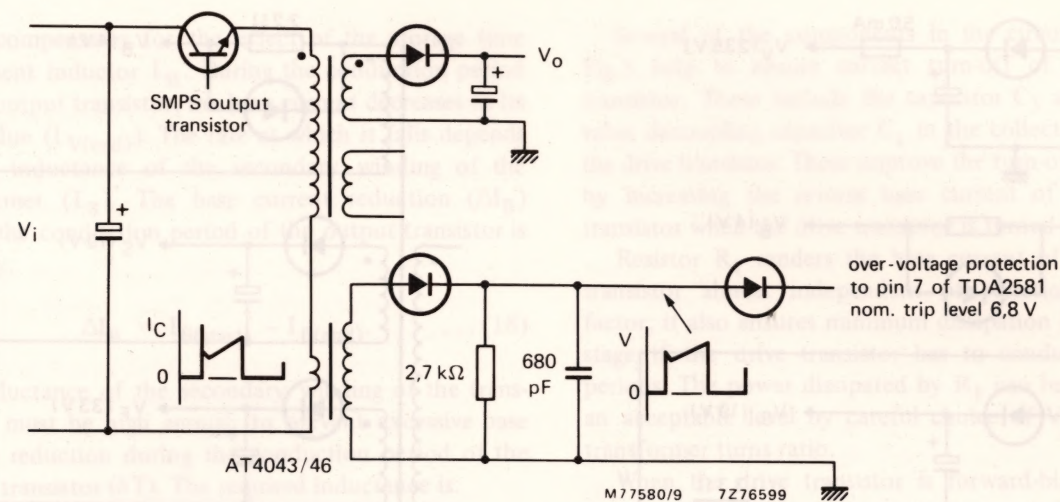


Fig.9 — An optional circuit for sensing the peak collector current of the SMPS output transistor with a current transformer (type AT4043/46)

INTERFERENCE SUPPRESSION

The high-frequency switching of an SMPS, and the presence of high-level alternating voltage and currents, cause some interference. The interference can be categorised as follows.

- 1) **Visible interference.** Visible interference is caused by the injection of spurious radiated signals into the tuner and i.f. amplifier circuits (or both) of the receiver. The main source of visible interference is the fast rate of change (dI/dt) of the current pulses passed by the switching transistors and diodes.
- 2) **Symmetrical mains pollution.** Symmetrical mains interference appears between the mains input lines, and is caused by the SMPS switching currents through the equivalent series resistance ESR of the input capacitor.
- 3) **Asymmetrical mains pollution.** Asymmetrical mains interference appears between earth and each of the mains lines. It is caused by the currents that flow through the capacitance between earth and the components that carry high-level a.c. voltages. This type of interference is more pronounced in mains-isolated supplies because of the high impedance between the primary and secondary windings of the output transformer.

Symmetrical and asymmetrical interference are interactive and thus it is usually necessary to take steps to reduce both, as the reduction of one might increase the other.

Reduction of interference

The collector of the SMPS output transistor must be connected to a constant potential to prevent short-rise-time current flowing into the stray capacitance at the collector. A capacitor must be connected in parallel with the primary winding of the output transformer, to reduce

the loop in which the high rate of change of transformer current occurs. A low-value low-inductance resistor can be connected in series with the capacitor to damp current oscillations.

The rate of change of voltage (dV/dt) across the diodes in the secondary winding circuits can be decreased by connecting a capacitor in parallel with each diode.

The rate of change of voltage at the driver transformer should be decreased by a CR network (470 pF and 56 Ω) connected in the collector circuit of the driver transistor.

When designing the printed-wiring board, certain circuit loops should be kept as short as possible. These are:

- 1) the circuit comprising the input electrolytic capacitor, the SMPS output transistor, and the primary winding of the output transformer;
- 2) the circuit comprising the main secondary winding of the output transformer, the flywheel diode, and the output electrolytic capacitor;
- 3) the circuit loops containing the damping components.

Reduction of mains pollution

The most obvious precaution against mains pollution is to position the mains rectification circuit where it is least affected by the electrostatic and electromagnetic fields generated by the primary and secondary circuits of the output transformer. Apart from this, there are several precautions which should be taken.

A capacitor must be connected in parallel with each diode of the mains rectifier bridge to act as a snubber (reducing the h.f. component of the diode current waveform). A filter choke should be connected in series with the mains lines and a capacitor (class-X) should be connected between them. The most effective type of filter choke is one which consists of two windings on a closed core. The windings are then mutually coupled so

that the mains currents generate opposing fields. Two shields incorporated in the output transformer will prevent a.c. voltages appearing between the primary and the secondary windings. Finally, a capacitor should be connected between the mains-isolated and non-isolated common return rails. Safety regulations specify a class-Y capacitor, and its value should not exceed 4.7 nF.

Reduction of visible interference

The measures already described reduce the overall interference level in the SMPS, and reduce the mains pollution in the frequency range 0.16 to 1.6 MHz. Visible interference is caused by radiated r.f. signals within the tuning range of the receiver. This interference is most noticeable at the lower end of the v.h.f. band, especially when the input signal is weak and a set-top aerial is used.

Visible interference appears as vertical black stripes on the screen when the SMPS is synchronised with the line frequency. The various sources of visible interference are shown in Fig.10. The voltage sources E are generated by r.f. current in earth loops on the printed-wiring board, and may be minimised by careful attention to the board layout design as already described. The voltage E_{S1} is caused by diode current pulses flowing through the r.f. impedance of C_1 . The current flowing in the SMPS output circuit due to E_{S1} gives rise to an r.f. voltage source E' within the current loop shown in Fig.10. The cause of E_{S2} is bad decoupling of the bridge rectifier.

Since the mains is effectively at earth potential at high frequencies, a current loop exists as shown in Fig.10, with the result that an interference voltage is generated across the 75 Ω input impedance of the tuner.

Besides careful design of the printed-wiring board layout, several additional measures can be taken to

minimise this visible interference. The capacitor at SMPS outputs should have a low r.f. impedance so that voltages such as E_{S1} are reduced. The connection of the safety capacitor is also important as this can be connected in such a manner that the major sources of induced interference (E and E') are excluded from the interference current loop, as shown in Fig.11. The influence of such sources of interference as E_{S1} and E_{S2} can be reduced by connecting LC filters in the output lines of the SMPS and in series with the mains input (see Fig.11). The voltage from source E_{S1} can also be reduced by connecting inductor L' in series with the diode. This inductor also reduces the collector current of the SMPS switching transistor at turn-on by limiting the inrush current in the output capacitor.

CIRCUIT DESCRIPTION

Figs.12 and 13 give the complete circuit of a mains-isolated SMPS using a flyback d.c.-to-d.c. converter and a control IC type TDA2581 (Ref.2).

Mains input circuit

An LC filter in the mains input lines suppresses SMPS-generated noise. Even without a screening can for the SMPS, this limits the mains pollution to about 10 dB below the CISPR (No.13) limits.

Mains is also applied to a small transformer for supplying standby power for a remote-controlled receiver. The transformer output is full-wave rectified and smoothed by a capacitive filter to provide a 35V mains-isolated supply. This supply is also used to power the control IC and the driver stage. This arrangement has a number of advantages over the circuit shown in a previous article (Ref.1) where the control IC is powered from the main

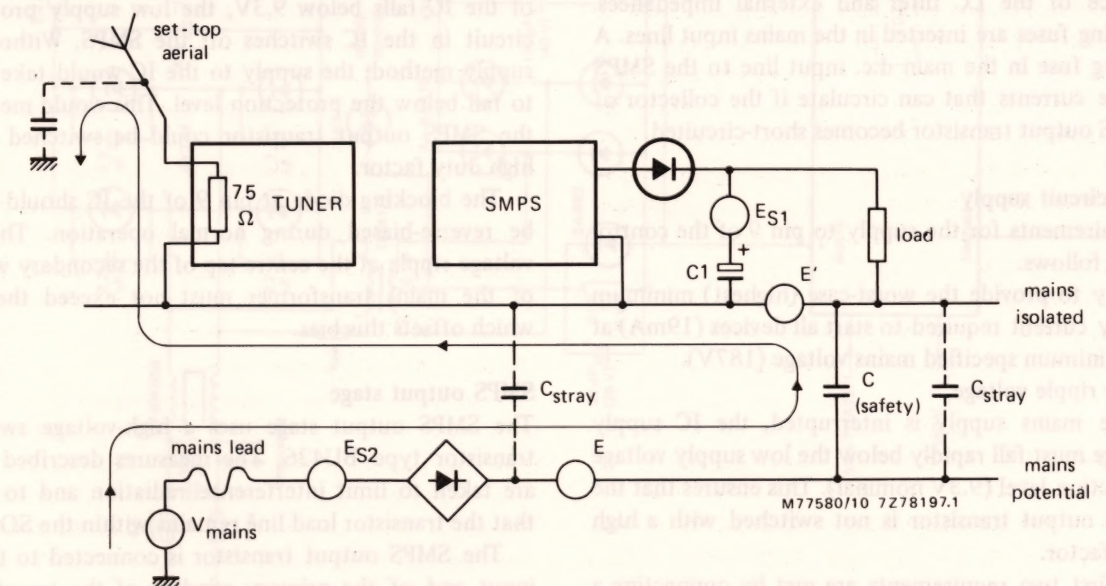


Fig.10 — Earth loop current in tv receiver. Mains input is at earth potential for r.f. signals

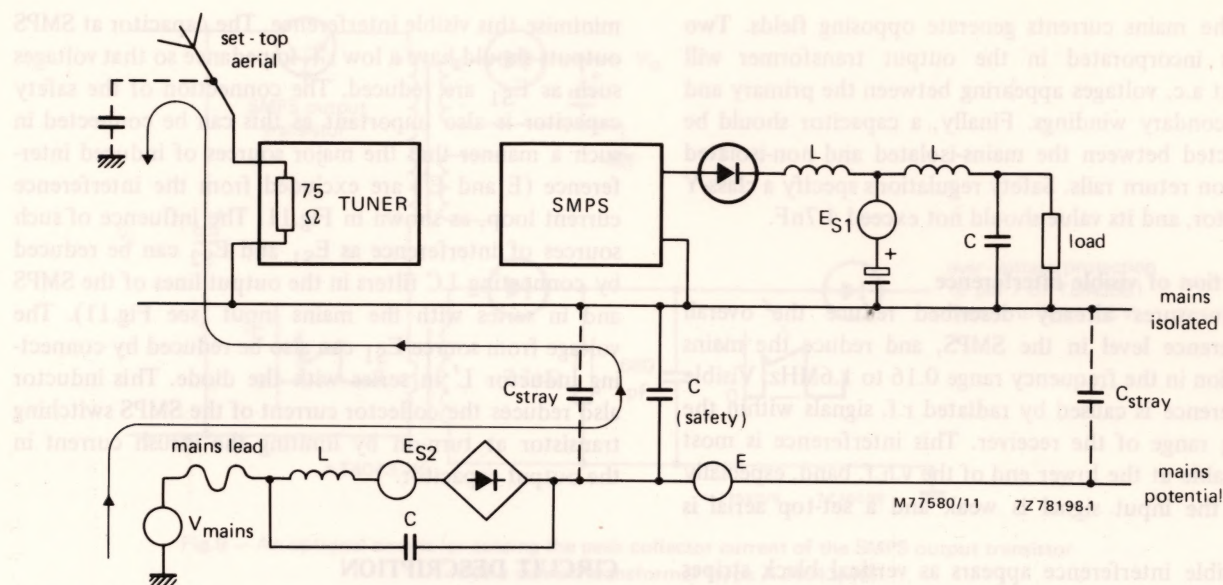


Fig.11 – Visible interference is reduced with the use of filters and the repositioning of the safety capacitor

d.c. (non-isolated) input of the SMPS. The advantages are:

- 1) mains isolation is required only between the windings of the standby supply transformer, the drive transformer, and the output transformer;
- 2) voltage stabilisation is improved because the regulation is not a function of the coupling between the windings of the output transformer;
- 3) there is very little dissipation in bleeder resistors.

The mains input is also applied to a bridge rectifier type BY224, the output from which is smoothed by a capacitive filter to provide the main d.c. input to the SMPS. The peak inrush current drawn from the mains is limited by a 2.2Ω resistor in conjunction with the impedance of the LC filter and external impedances. Slow-acting fuses are inserted in the mains input lines. A fast-acting fuse in the main d.c. input line to the SMPS limits the currents that can circulate if the collector of the SMPS output transistor becomes short-circuited.

Control circuit supply

The requirements for the supply to pin 9 of the control IC are as follows.

- 1) Ability to provide the worst-case (highest) minimum supply current required to start all devices (19mA) at the minimum specified mains voltage (187V).
- 2) A low ripple voltage.
- 3) If the mains supply is interrupted, the IC supply voltage must fall rapidly below the low supply voltage protection level (9.3V nominal). This ensures that the SMPS output transistor is not switched with a high duty factor.

The first two requirements are met by connecting a voltage regulator diode (11V) and a 1k Ω resistor across

the 35V supply, and connecting their junction to pin 9 of the IC.

The last requirement is met by connecting a 510 Ω resistor and a 22 μ F capacitor between the common return and the centre-tap of the secondary of the mains transformer. The voltage across this network decreases rapidly as the network has a low CR product. The network is connected to pin 9 of the IC via a diode which is reverse-biased during normal operation; the supply for the IC is derived from the 35V supply line via the 1k Ω resistor. If the mains supply is interrupted for any reason, the voltage at the centre-tap of the secondary winding of the transformer falls rapidly, causing the diode to conduct. When the voltage at pin 9 of the IC falls below 9.3V, the low supply protection circuit in the IC switches off the SMPS. Without this supply method, the supply to the IC would take longer to fall below the protection level. This would mean that the SMPS output transistor could be switched with a high duty factor.

The blocking diode at pin 9 of the IC should always be reverse-biased during normal operation. Thus the voltage ripple at the centre-tap of the secondary winding of the mains transformer must not exceed the value which offsets this bias.

SMPS output stage

The SMPS output stage uses a high-voltage switching transistor type BU426. The measures described below are taken to limit interference radiation and to ensure that the transistor load line remains within the SOAR.

The SMPS output transistor is connected to the d.c. input end of the primary winding of the transformer. This arrangement reduces the rate of change of current

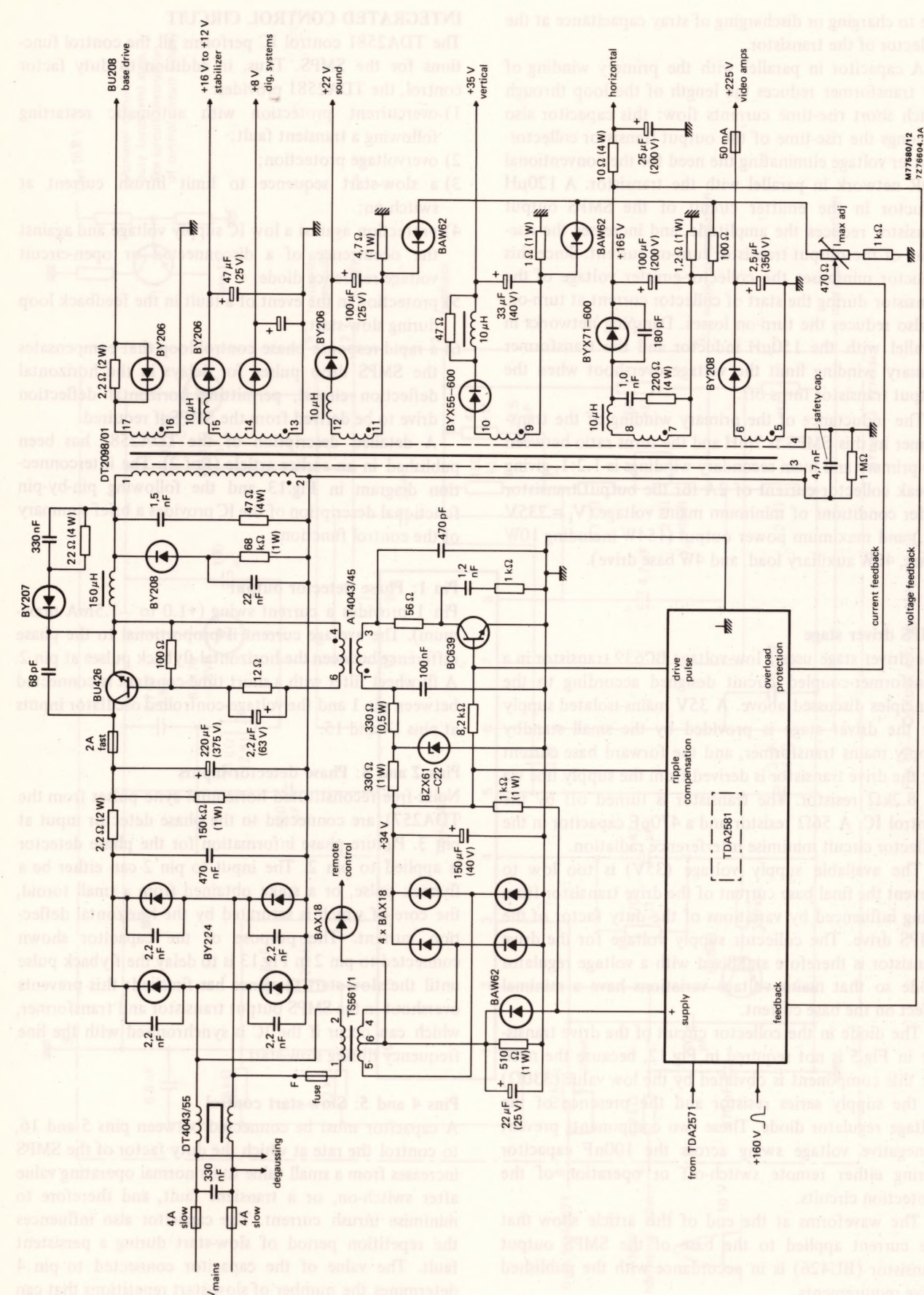


Fig. 12 — Flyback converter SMPS for providing mains-isolated power supplies and horizontal deflection drive for a ctv receiver

due to charging or discharging of stray capacitance at the collector of the transistor.

A capacitor in parallel with the primary winding of the transformer reduces the length of the loop through which short rise-time currents flow: this capacitor also prolongs the rise-time of the output transistor collector-emitter voltage eliminating the need for the conventional CDR network in parallel with the transistor. A $120\mu\text{H}$ inductor in the emitter circuit of the SMPS output transistor reduces the amplitude, and increases the rise-time, of the output transistor turn-on current. Since this inductor minimises the collector-emitter voltage of the transistor during the start of collector current at turn-on, it also reduces the turn-on losses. Damping networks in parallel with the $150\mu\text{H}$ inductor and the transformer primary winding limit the voltage overshoot when the output transistor turns off.

The inductance of the primary winding of the transformer in this SMPS is 7mH and the turns ratio between the primary and main secondary windings is 1.2:1, giving a peak collector current of 2A for the output transistor under conditions of minimum mains voltage ($V_i = 235\text{V}$ d.c.) and maximum power output (154W including 10W losses, 40W auxiliary load, and 4W base drive).

SMPS driver stage

The driver stage uses a low-voltage BC639 transistor in a transformer-coupled circuit designed according to the principles discussed above. A 35V mains-isolated supply for the driver stage is provided by the small standby supply mains transformer, and the forward base current for the drive transistor is derived from the supply line via an $8.2\text{k}\Omega$ resistor. The transistor is turned off by the control IC. A 56Ω resistor and a 470pF capacitor in the collector circuit minimise interference radiation.

The available supply voltage (35V) is too low to prevent the final base current of the drive transistor from being influenced by variations of the duty factor of the SMPS drive. The collector supply voltage for the drive transistor is therefore stabilised with a voltage regulator diode so that mains voltage variations have a minimal effect on the base current.

The diode in the collector circuit of the drive transistor in Fig.5 is not required in Fig.12, because the need for this component is obviated by the low value (330Ω) of the supply series resistor and the presence of the voltage regulator diode. These two components prevent a negative voltage swing across the 100nF capacitor during either remote switch-off or operation of the protection circuits.

The waveforms at the end of this article show that the current applied to the base of the SMPS output transistor (BU426) is in accordance with the published drive requirements.

INTEGRATED CONTROL CIRCUIT

The TDA2581 control IC performs all the control functions for the SMPS. Thus, in addition to duty factor control, the TDA2581 provides:

- 1) overcurrent protection with automatic restarting following a transient fault;
- 2) overvoltage protection;
- 3) a slow-start sequence to limit inrush current at switch-on;
- 4) protection against a low IC supply voltage and against the occurrence of a disconnected or open-circuit voltage reference diode;
- 5) protection in the event of a fault in the feedback loop during slow-start;
- 6) a rapid-response phase control loop that compensates the SMPS drive pulses for delays in the horizontal deflection circuit, permitting horizontal deflection drive to be derived from the SMPS if required.

A detailed description of the TDA2581 has been published in an earlier article (Ref.2). The interconnection diagram in Fig.13 and the following pin-by-pin functional description of the IC provides a brief summary of the control functions.

Pin 1: Phase detector output

Pin 1 provides a current swing ($+1.0$ to -1.5mA maximum). The average current is proportional to the phase difference between the horizontal flyback pulses at pin 2. A flywheel filter with a short time-constant is connected between pin 1 and the voltage-controlled oscillator inputs at pins 14 and 15.

Pins 2 and 3: Phase detector inputs

Noise-free reconstituted horizontal sync pulses from the TDA2571 are connected to the phase detector input at pin 3. Picture phase information for the phase detector is applied to pin 2. The input to pin 2 can either be a flyback pulse, or a spike obtained from a small toroid, the core of which is saturated by the horizontal deflection current. The purpose of the capacitor shown connected to pin 2 in Fig.13 is to delay the flyback pulse until the slow-start sequence has finished: this prevents overshoot in the SMPS output transistor and transformer, which can occur if the IC is synchronised with the line frequency during slow-start.

Pins 4 and 5: Slow-start control

A capacitor must be connected between pins 5 and 16, to control the rate at which the duty factor of the SMPS increases from a small value to its normal operating value after switch-on, or a transient fault, and therefore to minimise inrush current. The capacitor also influences the repetition period of slow-start during a persistent fault. The value of the capacitor connected to pin 4 determines the number of slow-start repetitions that can

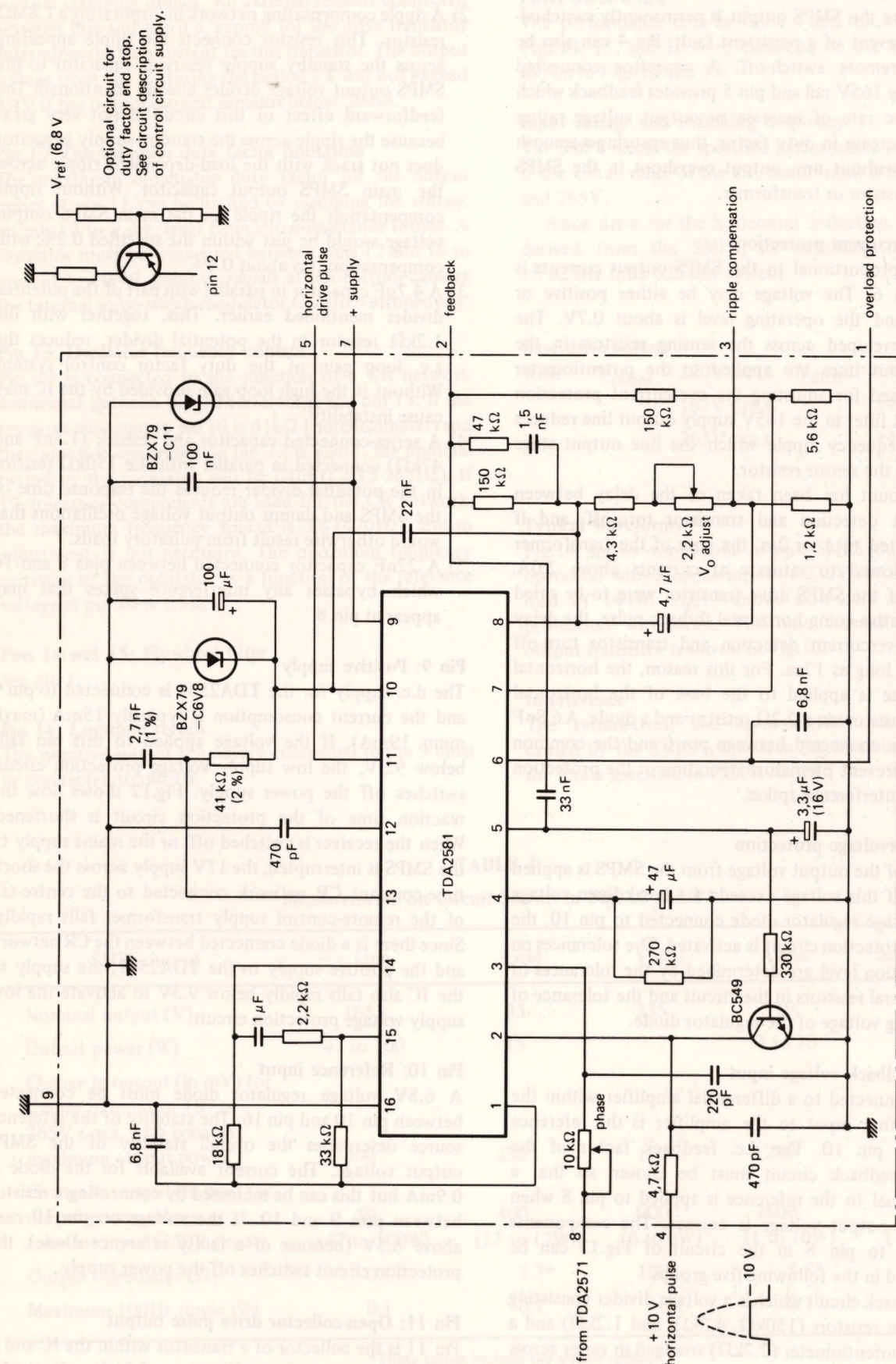


Fig.13 - Control sub-assembly circuit

occur before the SMPS output is permanently switched-off in the event of a persistent fault. Pin 4 can also be used for remote switch-off. A capacitor connected between the 165V rail and pin 5 provides feedback which controls the rate of increase in output voltage rather than the increase in duty factor, thus ensuring a smooth slow-start without any output overshoot in the SMPS output transistor or transformer.

Pin 6: Overcurrent protection

A voltage proportional to the SMPS output currents is fed to pin 6. The voltage may be either positive or negative, and the operating level is about 0.7V. The voltages developed across the sensing resistors in the SMPS output lines are applied to the potentiometer which is used for adjusting the overcurrent protection level. A CR filter in the 165V supply output line reduces the line frequency ripple which the line output stage imposes on the sensor resistor.

No account has been taken of the delay between overcurrent detection and transistor turn-off, and if this is limited to 1 or 2 μ s, the core of the transformer can be allowed to saturate at currents above 2.0A. However, if the SMPS drive transistor were to be gated with a negative-going horizontal flyback pulse, the delay between overcurrent detection and transistor turn-off may be as long as 12 μ s. For this reason, the horizontal gating pulse is applied to the base of the horizontal output transistor via a 2.2 Ω resistor and a diode. A 6.8nF capacitor is connected between pin 6 and the common return to prevent premature operation of the protection circuit by interference spikes.

Pin 7: Overvoltage protection

A sample of the output voltage from the SMPS is applied to pin 7. If this voltage exceeds the breakdown voltage of the voltage regulator diode connected to pin 10, the overload protection circuit is activated. The tolerances on the protection level are determined by the tolerances of the peripheral resistors in the circuit and the tolerance of the working voltage of the regulator diode.

Pin 8: Feedback voltage input

Pin 8 is connected to a differential amplifier within the IC. The other input to the amplifier is the reference voltage at pin 10. The d.c. feedback factor of the external feedback circuit must be chosen so that a voltage equal to the reference is applied to pin 8 when the SMPS output voltage is correct. The components connected to pin 8 in the circuit of Fig.13 can be summarised in the following five groups.

- 1) A feedback circuit which is a voltage divider consisting of three resistors (150k Ω , 4.3k Ω , and 1.2k Ω) and a preset potentiometer (2.2k Ω) arranged in series across the SMPS main output.

- 2) A ripple compensating network incorporating a 1.8M Ω resistor. This resistor connects the ripple appearing across the standby supply reservoir capacitor to the SMPS output voltage divider already mentioned. The feedforward effect of this circuit is not very great because the ripple across the standby supply capacitor does not track with the load-dependent ripple across the main SMPS output capacitor. Without ripple compensation the ripple on the main SMPS output voltage would be just within the specified 0.2%; with compensation it is about 0.1%.
- 3) A 4.7 μ F capacitor in parallel with part of the potential divider mentioned earlier. This, together with the 1.2k Ω resistor in the potential divider, reduces the a.c. loop gain of the duty factor control system. Without it the high loop gain provided by the IC may cause instability.
- 4) A series-connected capacitor and resistor (1.5nF and 47k Ω) connected in parallel with the 150k Ω resistor in the potential divider reduces the response time of the SMPS and damps output voltage oscillations that would otherwise result from pulsatory loads.
- 5) A 22nF capacitor connected between pins 8 and 10 which bypasses any interference spikes that may appear at pin 8.

Pin 9: Positive supply

The d.c. supply for the TDA2581 is connected to pin 9 and the current consumption is typically 15mA (maximum 19mA). If the voltage applied to this pin falls below 9.3V, the low supply voltage protection circuit switches off the power supply. Fig.12 shows how the reaction time of the protection circuit is shortened. When the receiver is switched off, or the mains supply to the SMPS is interrupted, the 17V supply across the short-time-constant CR network connected to the centre-tap of the remote-control supply transformer falls rapidly. Since there is a diode connected between the CR network and the positive supply to the TDA2581, the supply to the IC also falls rapidly below 9.3V to activate the low supply voltage protection circuit.

Pin 10: Reference input

A 6.8V voltage regulator diode must be connected between pin 10 and pin 16. The stability of the reference source determines the overall stability of the SMPS output voltage. The current available for the diode is 0.9mA but this can be increased by connecting a resistor between pins 9 and 10. If the voltage on pin 10 rises above 8.5V (because of a faulty reference diode), the protection circuit switches off the power supply.

Pin 11: Open-collector drive pulse output

Pin 11 is the collector of a transistor within the IC and is protected against the application of high voltages by

internal clamping diodes. An external resistor connected between this and the d.c. supply for the drive transistor determines the base current for this transistor. The output voltage from pin 11 during the period δT will not exceed 0.4V if the output current remains below 20mA.

Pin 12: Output-pulse duty factor limitation

The maximum obtainable duty factor for the output pulses at pin 11 can be limited by clamping the voltage on pin 12 to a d.c. level from a low-resistance source. A capacitor must be connected between pins 12 and 16 to prevent low-level spurious signals at pin 8 from causing the internal pulse-width modulator to switch erroneously.

Pin 13: Oscillator frequency control

Pin 13 is connected to the junction of a CR network connected between pin 10 (reference) and pin 13. If the resistor connected to pin 10 is 41k Ω (potentiometer) and the capacitor connected to pin 13 is 2.7nF, the nominal period of the oscillator will be 64 μ s ($f = 15.265$ Hz). If 1% tolerance components are used for the CR network, the maximum frequency spread is 3% (470Hz), and so adjustment is not necessary. The maximum frequency variation of the oscillator as a function of the reference voltage at pin 10 is 1.5%/V.

Pins 14 and 15: Flywheel filter

See pin 1.

Pin 16: Common return

The negative side of the supply connected to pin 9 must be connected to pin 16.

PERFORMANCE

The performance data in Table 4 and the waveforms in Figs.14, 15, and 16 were measured on the SMPS circuit shown in Figs.12 and 13.

Input voltage and switching frequency

The SMPS meets the specified performance requirements if the r.m.s. value of the a.c. mains input is between 187 and 265V.

Since drive for the horizontal deflection transistor is derived from the SMPS, its switching frequency is 15.625Hz for a 625-line system.

Base drive voltage

With: $V_{\text{mains}} = 220\text{V r.m.s.}$ $V_{\text{drive}} = +4.4$ to -6.4V
 187V r.m.s. +4.4 to -5.6V
 265V r.m.s. +4.4 to -7.6V

Typical waveforms

Fig.14 shows waveforms of the SMPS during normal operation with a mains input of 220V r.m.s. and a total load of 144W. Fig.15 shows slow-start and overload protection waveforms. The base current of the line output transistor is shown in Fig.16.

Interference

The symmetrical and asymmetrical mains pollution caused by the SMPS is shown in Fig.17 to be well within the limits specified in CISPR No.13.

TABLE 4
Measurements on Circuit Shown in Figs.12 and 13

SMPS output	Line	Field	Video	Audio	Small-signal
Nominal output (V)	165	33	235	19	16
Output power (W)	47 to 100	15	7	1 to 10	8
Change in output (in mV) for change in input of 187 to 265V r.m.s. with constant					
maximum output power	300	230	170	270	240
Change in output (in mV) for output power change at constant input (220V r.m.s.)	50 (47 to 100W)	460 (13 to 17W)	900 (6 to 8W)	2600 (1 to 10W)	280 (7 to 9W)
Output impedance (Ω)	0.17	3.7*	100	5.8*	2.2*
Maximum 100Hz ripple (%)	0.1	0.1	0.1	0.1	0.1

*These values include the sensor resistor

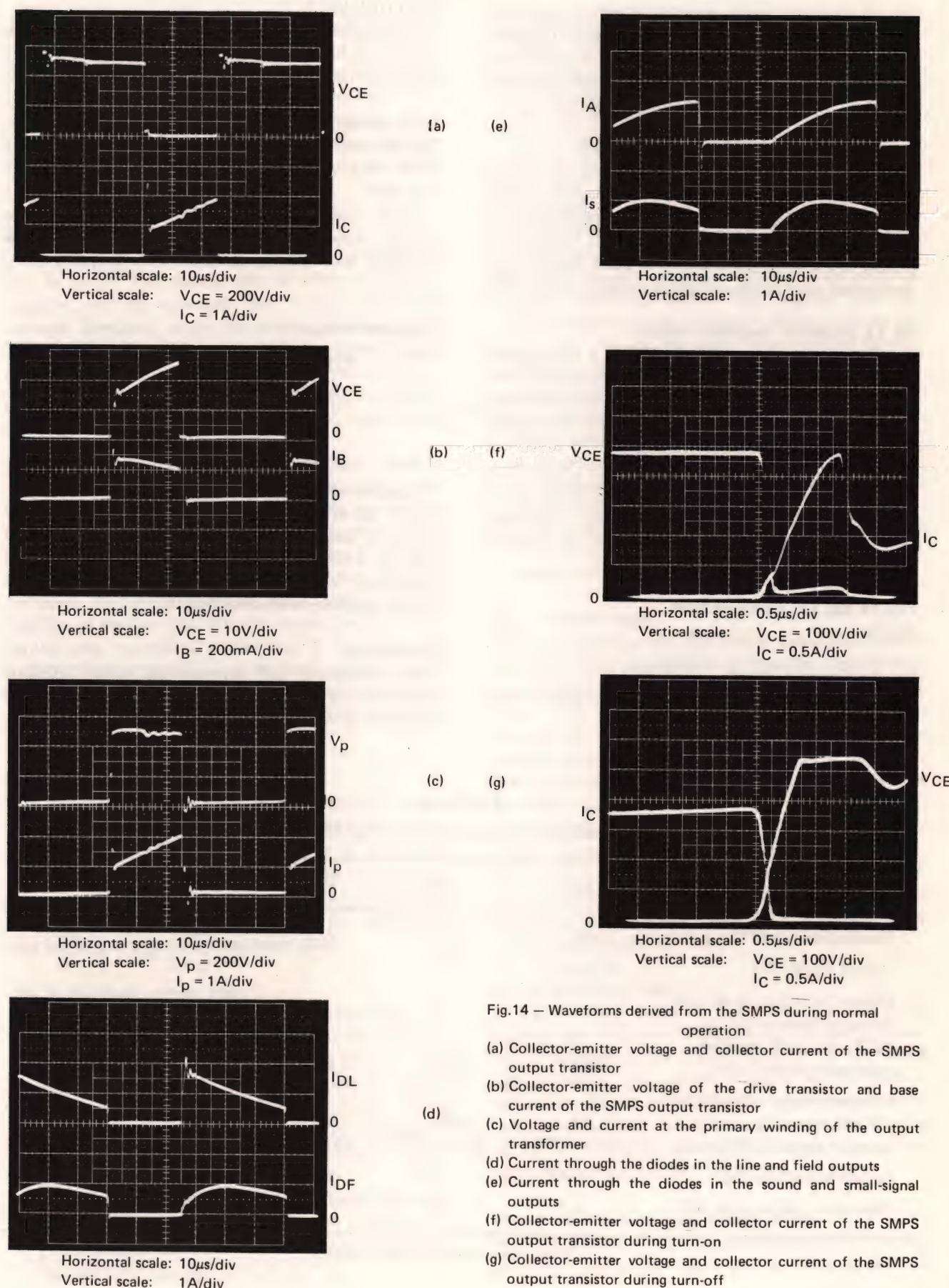


Fig.14 — Waveforms derived from the SMPS during normal operation

- (a) Collector-emitter voltage and collector current of the SMPS output transistor
- (b) Collector-emitter voltage of the drive transistor and base current of the SMPS output transistor
- (c) Voltage and current at the primary winding of the output transformer
- (d) Current through the diodes in the line and field outputs
- (e) Current through the diodes in the sound and small-signal outputs
- (f) Collector-emitter voltage and collector current of the SMPS output transistor during turn-on
- (g) Collector-emitter voltage and collector current of the SMPS output transistor during turn-off

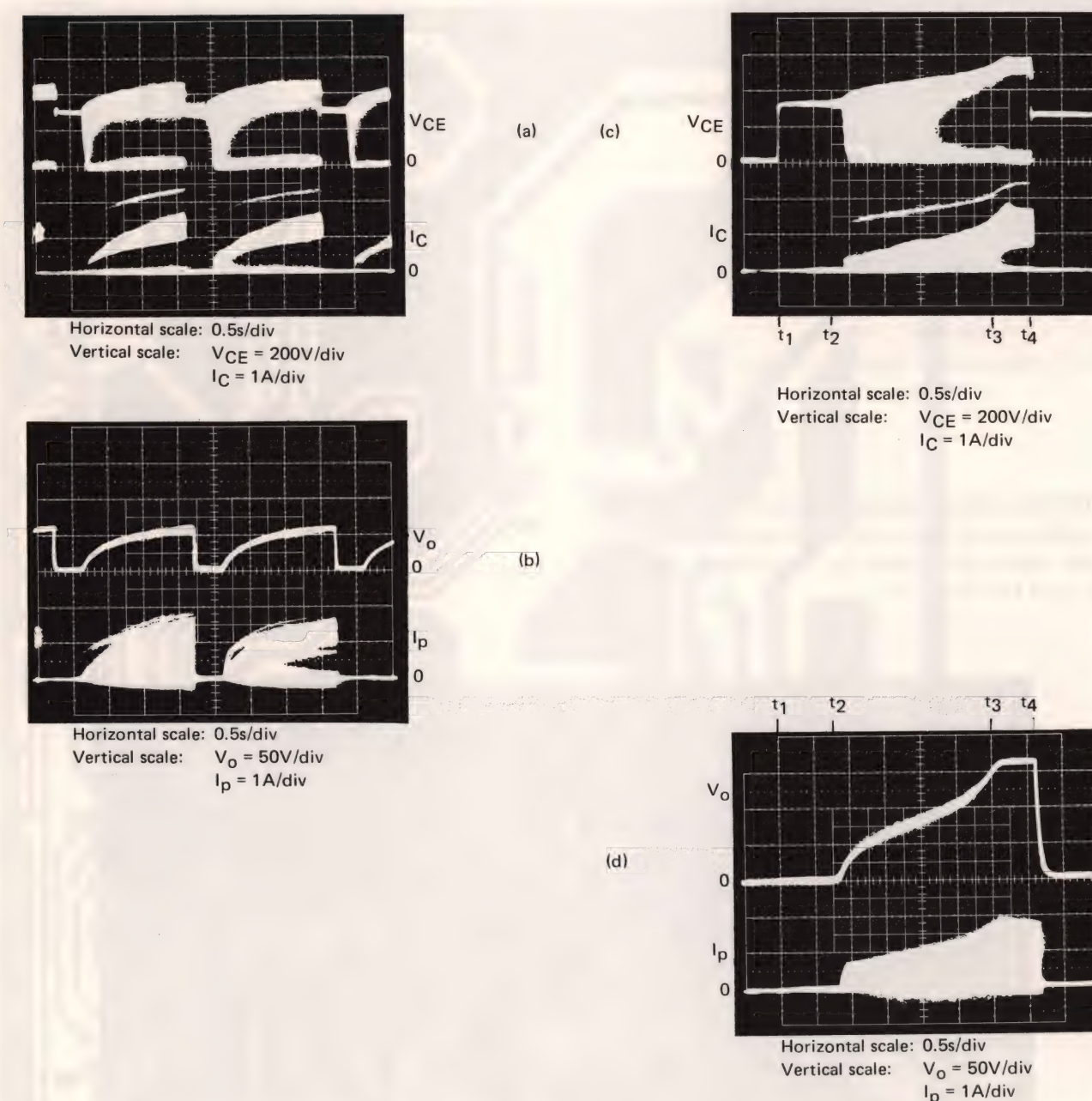
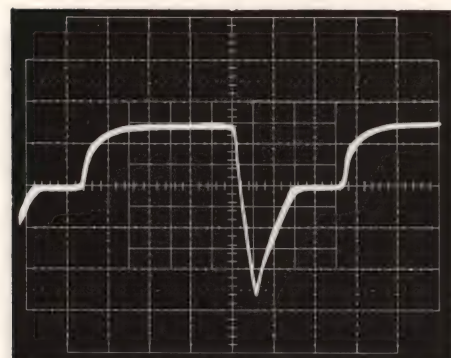


Fig.15 — Waveforms showing the operation of the overload protection and slow-start circuits in the TDA2581

- (a) Collector-emitter voltage and collector current of the SMPS output transistor operating in the 'hiccup mode' because of an overload on the main output
- (b) Main output voltage and the current through the primary winding of the output transformer when the SMPS is operating in the hiccup mode caused by an overload on the main output
- (c) Collector-emitter voltage and collector current of the SMPS output transistor during slow-start ($t_1 - t_3$) and normal operation ($t_3 - t_4$). The interval ($t_1 - t_2$) is the dead time of the control IC
- (d) Main output voltage and the current through the primary winding of the output transformer during slow-start ($t_1 - t_3$), normal operation ($t_3 - t_4$), and at switch-off (t_4). The interval ($t_1 - t_2$) is the dead time of the control IC



Horizontal scale: 10µs/div
Vertical scale: 1A/div
Fig.16 — Base current of line output transistor,
for $V_{\text{mains}} = 220\text{V}$

PRINTED-WIRING BOARD LAYOUT

A printed-wiring board meeting the layout requirements given earlier, and suitable for the circuit of Fig.12, is shown in Figs.18 and 19.

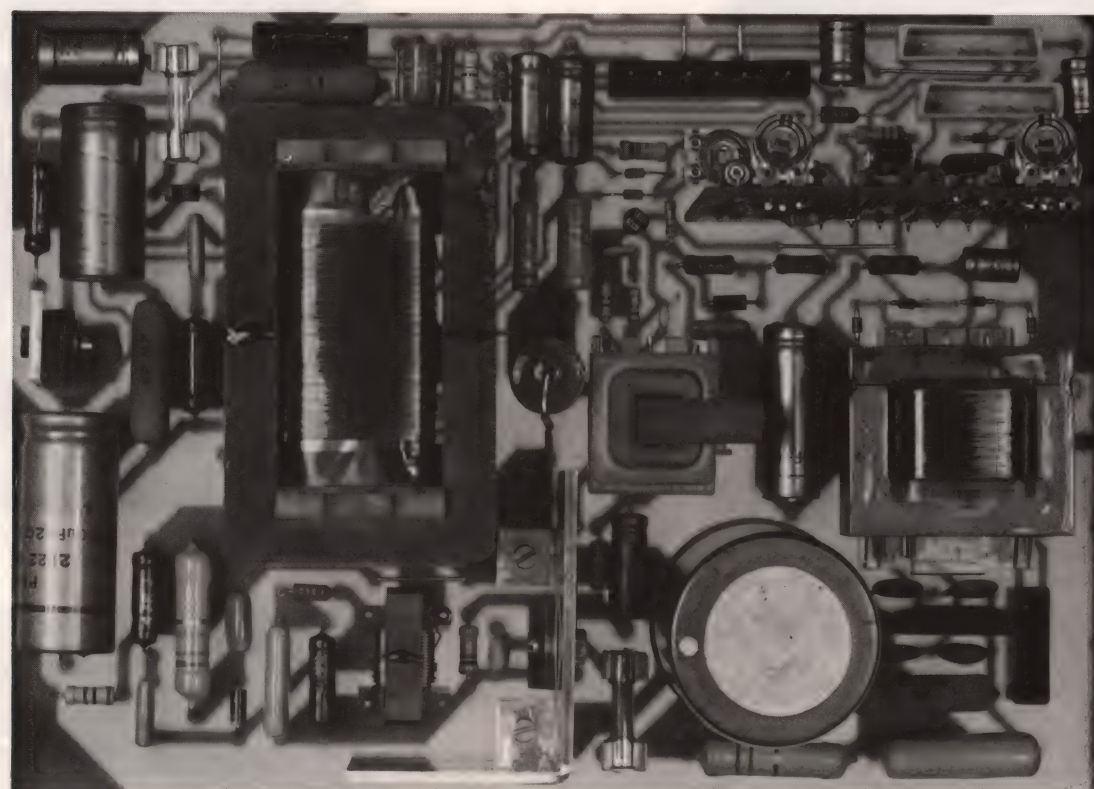


Fig.18 — Component side of the printed-wiring board (actual size)

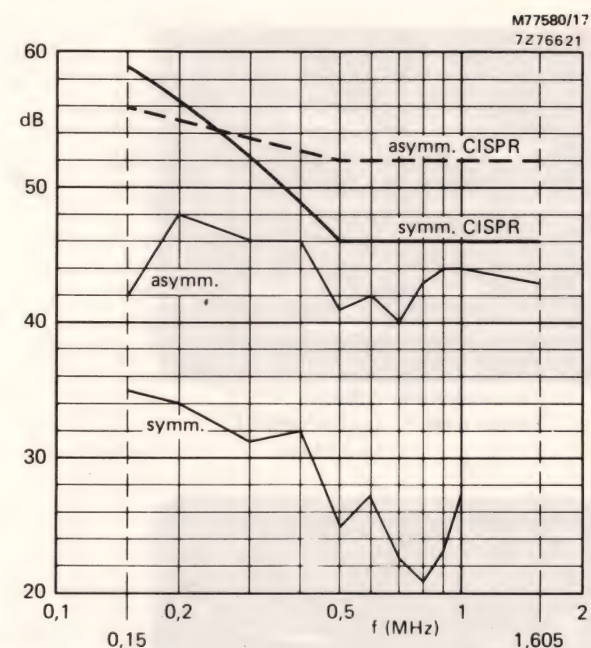


Fig.17 — Mains pollution caused by the SMPS compared with the CISPR (No.13) limits

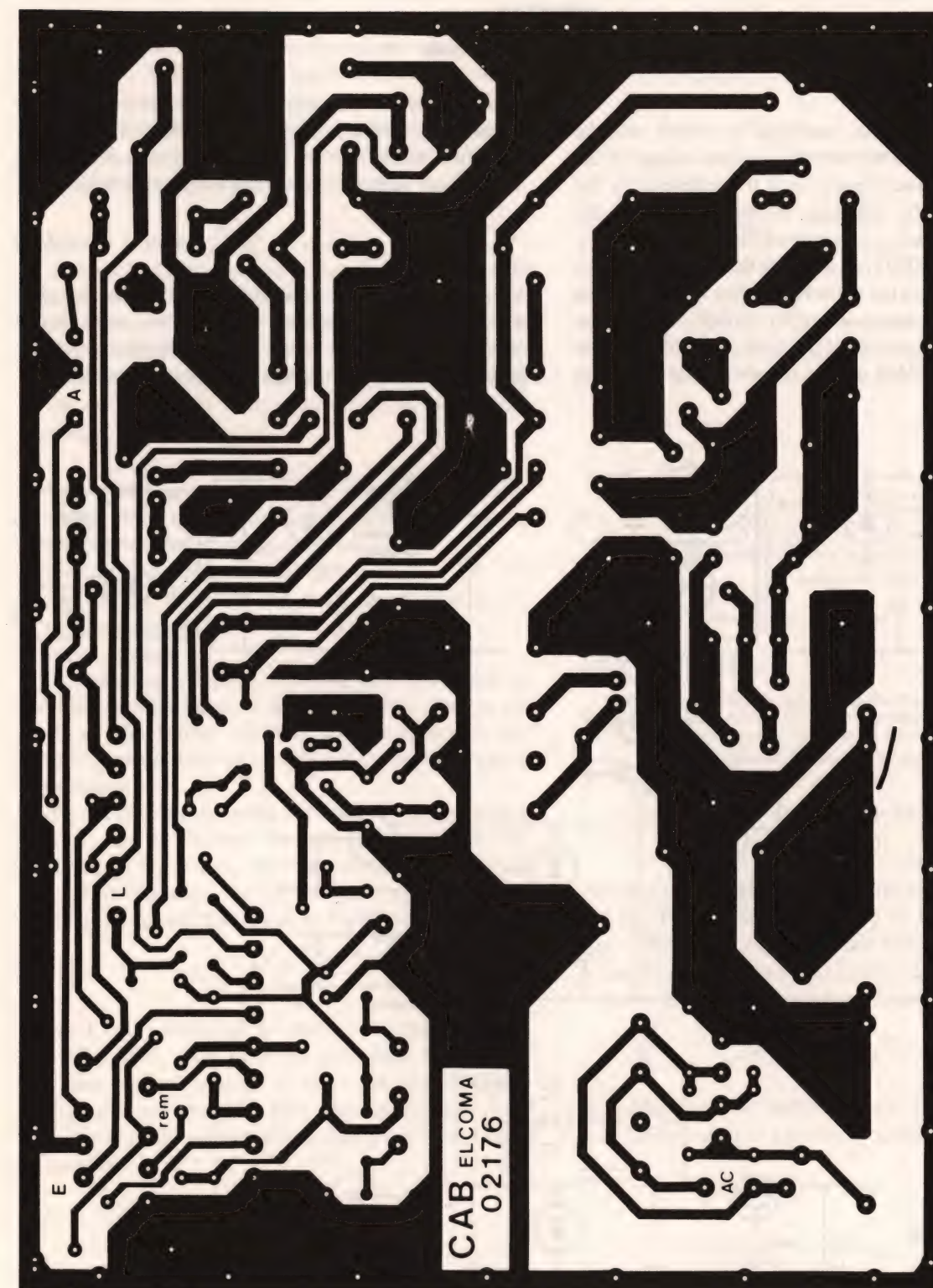


Fig.19 — Copper side of the printed-wiring board (actual size)

APPENDIX

Reducing Switching Losses

TURN-OFF LOSSES

When the SMPS output transistor is turned off, the inductive load causes the collector-emitter voltage of the transistor to increase rapidly until it is clamped by the flywheel diode. To minimise the turn-off losses, the slope of the increasing collector-emitter voltage must be limited to about $1000\text{V}/\mu\text{s}$, allowing the collector current to fall to zero before the collector-emitter voltage reaches a high value. The collector-emitter voltage rise-time can be increased by connecting a damping capacitor either in parallel with the SMPS output transistor (Fig.20a) or in

parallel with the primary winding of the output transformer (Fig. 20b). If it is assumed that the entire collector current is taken over by the damping capacitor during the turn-off period, its minimum capacitance is given by:

$$C_{\min} = \frac{I_{CM}}{dV/dt} \quad \dots (18)$$

For a maximum peak collector current of 2A, this gives a minimum capacitance of 2nF. However, as explained later, the maximum value of the capacitor must be limited during turn-on of the SMPS output transistor.

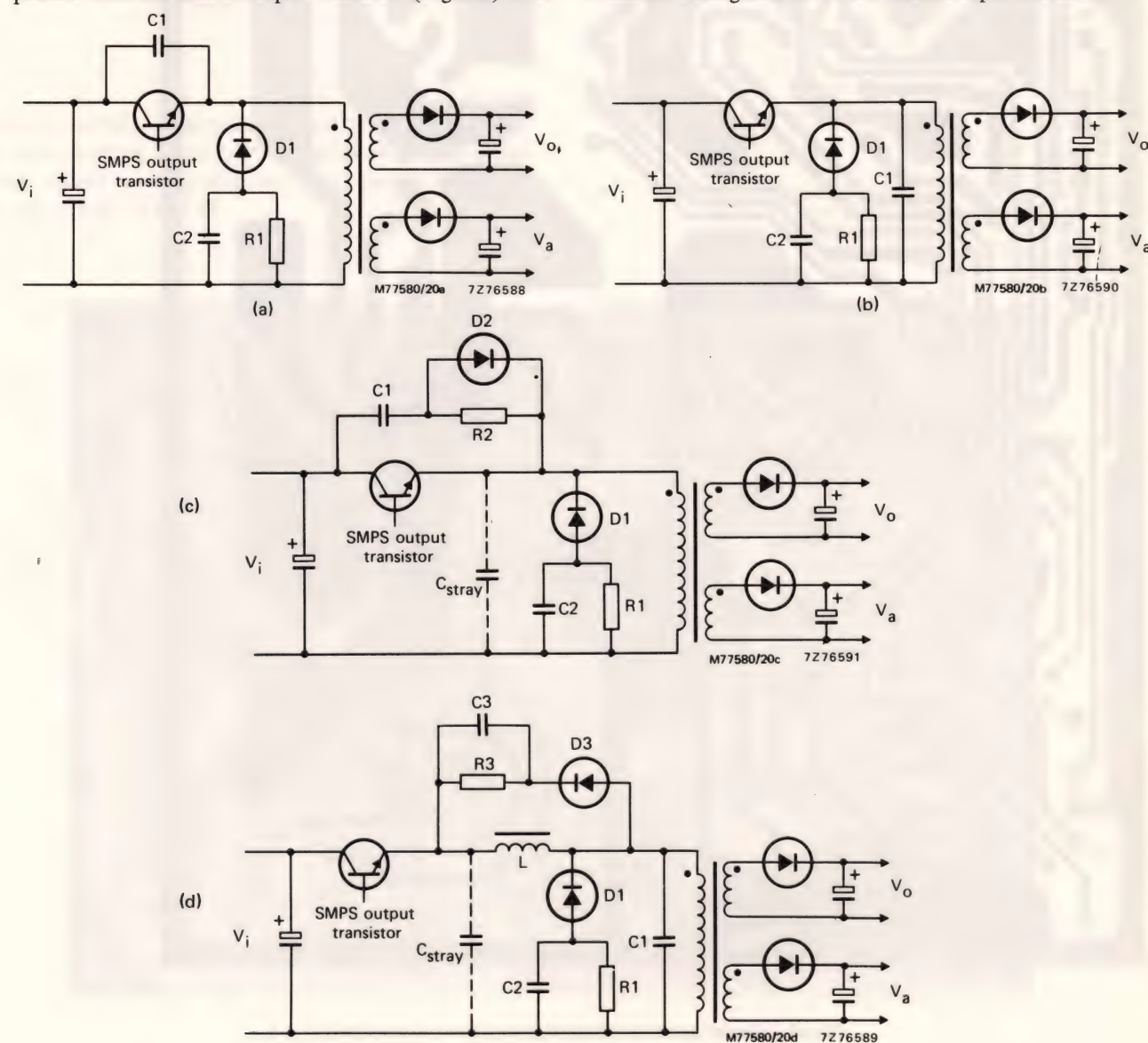


Fig.20 – Reducing switching losses in the SMPS output transistor
(a) and (b) damping capacitor to reduce turn-off losses
(c) and (d) network to prevent damping capacitor from causing high turn-off current

The leakage inductance of the transformer causes a voltage overshoot on the collector-emitter voltage waveform of the SMPS output transistor after turn-off. A voltage damping network (D_1 , C_2 , and R_1 in Fig.20b) can be used to prevent the collector-emitter voltage of the SMPS output transistor exceeding the collector-emitter breakdown voltage V_{CES} .

TURN-ON LOSSES

In a flyback d.c.-to-d.c. converter, the flywheel diode remains conducting until its entire current (including the reverse recovery charge) has been taken over by the SMPS output transistor. As shown in Fig.21, the following currents flow through the transistor, the currents flowing in the output diodes being transformed to the primary windings of the transformer.

- 1) the current necessary to remove the reverse recovery charge from the output diodes, transformed to the primary winding of the transformer;
- 2) the current to charge the damping capacitors;
- 3) the current to charge the stray capacitance in the emitter circuit of the transistor.

The resulting VA product during turn-on depends on the leakage inductance of the transformer, and on the levels of the various currents that contribute to the output transistor turn-on current and the applied turn-on base current.

To prevent the damping capacitor C_1 from causing a high turn-on current through the transistor, the components R_2 and D_2 must be connected as shown in Fig. 20c, or inductor L must be connected as shown in Fig. 20d. The power dissipation in R_2 is given by:

$$P_{\text{loss}} = \frac{C_1 V_{\text{CE}}^2}{2T}, \quad \dots (19)$$

where T is the period of the SMPS operating frequency. The value of C_1 must therefore be limited. The value of R_2 must be high enough to limit the peak discharge current, and low enough to fully discharge C_1 even if the duty factor of the transistor switching waveform is small. In practice:

$$C_1 \approx 2.2 \text{ nF},$$

and:

$$R_2 \simeq \frac{T}{10C_1} \Omega.$$

The circuit in Fig.20d has the advantage that the inductor allows the collector-emitter voltage of the transistor to reach a low value before the collector current has increased significantly. The inductor also prolongs the rise-time of the collector current, thereby

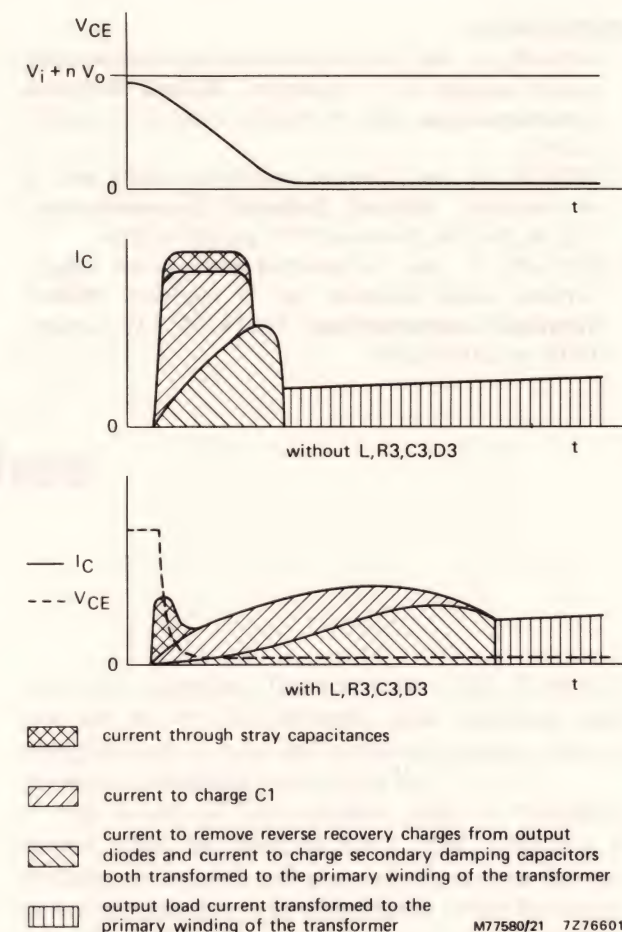


Fig.21 – Limiting the SMPS output transistor dissipation during turn-on

reducing its peak value shortly after turn-on. Oscillations in LC_1 after turn-on are damped by R_3 . All the energy stored in the inductor while the transistor is conducting is absorbed by R_2 via D_2 when the transistor turns off.

Since the inductor introduces losses given by:

$$P_{\text{loss}} = \frac{LI^2_{\text{CM}}}{2T}, \quad \dots (20)$$

its value must be limited. Good approximations for component values in a practical circuit are:

$$L = 150 \mu\text{H},$$

$$R_3 = \frac{10L}{T} \Omega,$$

$$C_3 = \frac{T}{10R_3} F.$$

In the specified circuit, $L = 150\mu\text{H}$, $R_3 = 22\Omega$, and $C_3 = 330\text{nF}$.

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Mullard Technical Communications, Vol.14, No.137,
January 1978

The photograph on the cover of this issue was stated to be of a secondary surveillance radar at London Heathrow. The picture in fact shows a Plessey AR1 primary radar. We apologise for this error.

Product Information: Plumbicon camera tubes

The Plumbicon* camera tube (Figs.1 and 2) was introduced by Philips in 1963 and is now accepted world-wide as the most suitable tube for high-quality colour television broadcasting. The range of available Plumbicon tubes also includes types for almost all industrial, medical, educational, and closed-circuit applications, as well as types to meet the rapidly increasing demands of

electronic journalism. Characteristics of the Plumbicon tube are its very fast response, good resolution, near-negligible dark current, and a spectral response close to the relative sensitivity curve of the eye.

Full details on the complete range of Plumbicon camera tubes are given in Ref.1. This publication is available on request, and gives information on the construction, operation, and performance of the Plumbicon tube. Detailed data on particular types is also available.

*Plumbicon is a registered trademark for camera tubes.



Fig.1 — XQ1410, XQ1080, and XQ1427 camera tubes

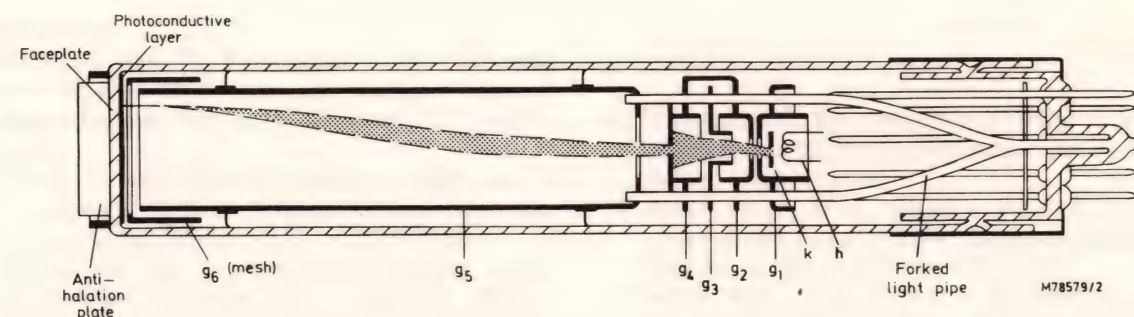


Fig.2 - Construction of a modern Plumbicon tube (XQ1080)

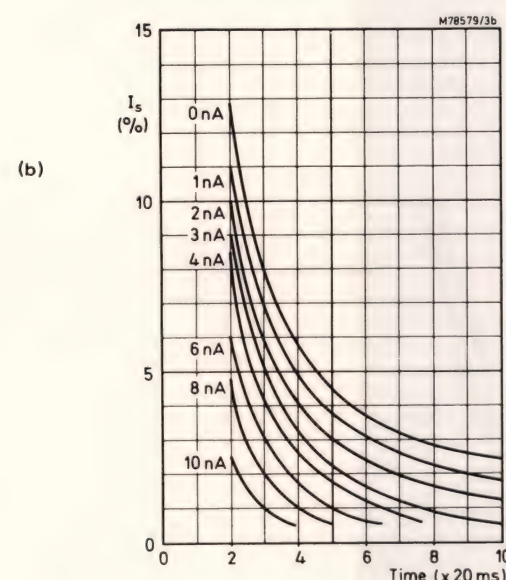
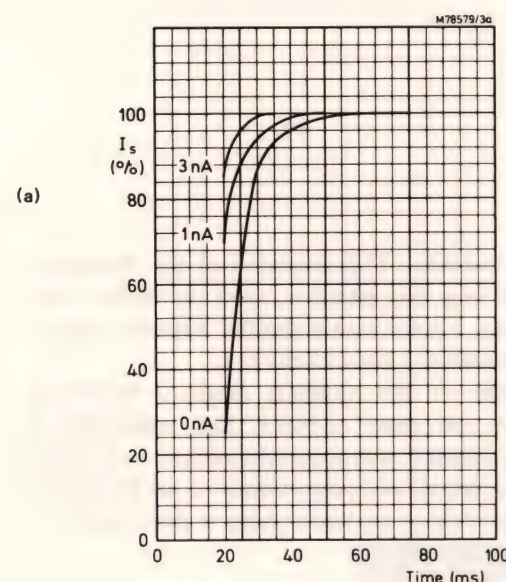


Fig.3 - Typical effect of bias lighting on lag in XQ1410 series tubes:
(a) build-up lag, measured after dark period of 10s
(b) decay lag (low-key conditions)

NEW DEVELOPMENTS

The latest tubes in the range for broadcasting applications are the 30mm XQ1410 series, which offers improvements over the standard XQ1020 series, and the 25mm XQ1500 series, which offers improvements over the XQ1080 series. In addition, ACT (anti-comet-tail) versions of the XQ1410 series, the XQ1520 series, will be available shortly. The 17.7mm XQ1427 and XQ1428 are intended for electronic journalism, industrial, and cable tv applications where small light-weight easy-to-operate cameras are required.

The XQ1410 series has improved resolution compared with the XQ1020 series; at 5MHz, the modulation depth of the XQ1410 is better by about 15%, on average an increase of from 40 to 55%. This improvement has been achieved by modifying the target layer.

The XQ1410 and XQ1520 series of tubes operate with light bias to minimise beam discharge lag. The non-uniformity of bias current across the target is typically about 10%. For colour cameras operating without black level shading correction, it is possible to use bias currents up to 5nA without noticeable background colour errors. If black level shading correction is applied (sawtooth and parabola), bias currents up to 10nA are permissible.

In both series the light bias can either be fixed or variable: for variable bias operation, the light bias lamp is externally driven; for fixed bias operation, an adaptor is provided which connects the bias lamp to the heater pins, via a resistor. The influence of bias lighting on lag in XQ1410 series tubes is shown in Fig.3.

Tubes of the XQ1500 series are interchangeable with the XQ1080 series tubes. However, they have an increased cathode rating (190mA compared with 95mA for the XQ1080 series) and a modified gun construction giving improved resolution.

The introduction of the 17.7mm XQ1427 tube makes possible the design of smaller colour cameras with sensitivity and speed of response approaching that of cameras fitted with standard 25 or 30mm tubes. This tube can also be used in industrial applications where, because of lag or dark current, a vidicon is not suitable. It has the same dimensions as 17.7mm vidicon or vidicon-

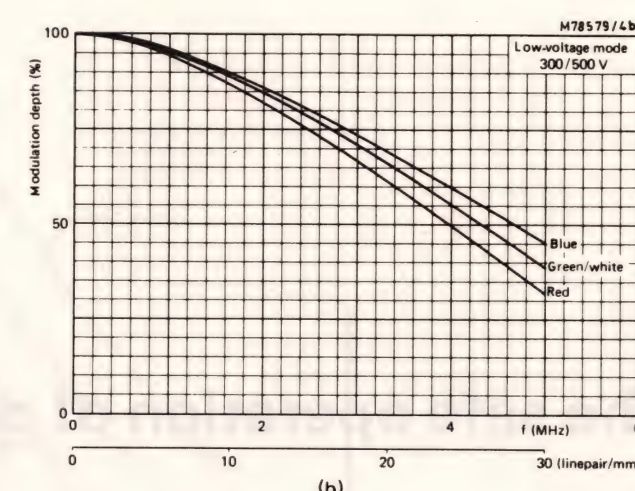
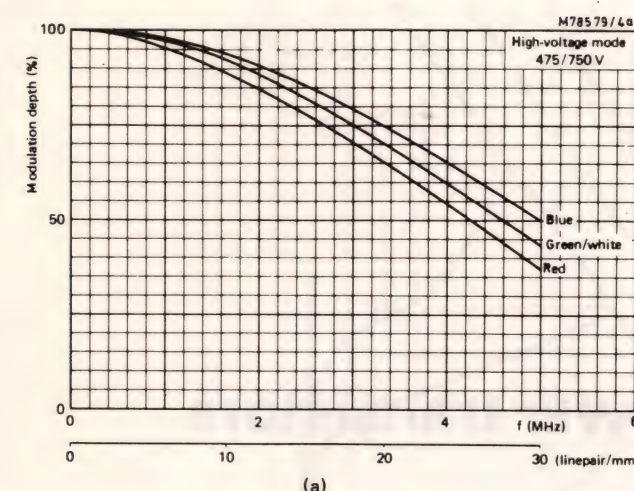


Fig.4 - Typical resolution characteristics of XQ1427 tube:
(a) high-voltage mode
(b) low-voltage mode

type tubes and is mechanically interchangeable with them.

Figs.4a and 4b show the typical resolution characteristics of the XQ1427 in white, red, green, and blue light. At 5MHz, the modulation depth in green light is typically 40%. The lag performance of the XQ1427 is excellent, the small size of the tube resulting in lower storage capacitance and hence reduced beam discharge lag.

REFERENCE

1. 'Plumbicon camera tubes', Technical Information 67, TP1662, Mullard Limited, 1978.

The safe operation of power transistors

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Mullard Technical Publications Department

This article describes and justifies the four limits to the Safe Operating Area (SOAR) of power transistors. The SOAR of a power transistor passing a direct current is then discussed because it forms the basis from which the SOARs for all other conditions are derived. Intermittent operation and the method of obtaining a SOAR for any type of waveform are considered, and high-voltage extensions to the SOAR are examined. Heat dissipation and the means of arriving at an appropriate heatsink are given extensive treatment. Finally, a flow chart is provided which can be used to check the suitability of a chosen transistor for a particular application.

INTRODUCTION

The principal ratings of power transistors are based upon maximum values of current, voltage, and power and temperature. The fourth main restriction in the operation of power transistors is the phenomenon known as second breakdown.

As an aid to the circuit designer, our published data contains safe operating areas for all types of power transistors. The safe operating area (SOAR) is a graph of collector current against collector-emitter voltage plotted on a log-log grid and has four boundaries: the current, voltage, power, and second breakdown limits, see Fig.1.

An understanding of the derivation of safe operating areas will not only help the circuit designer to use them, but also allow him to adapt them to particular circumstances.

The definitions of terms used in this article are given in Appendix 1.

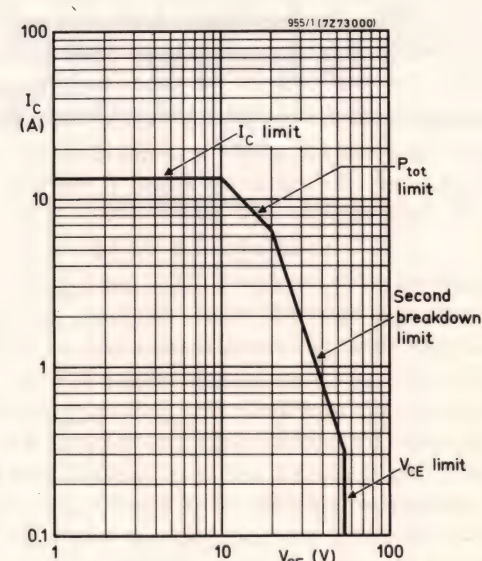


Fig.1 - A typical SOAR diagram with boundaries named

AVALANCHE BREAKDOWN

When a transistor is operated at a low collector current, such that $I_C V_{CE} \ll P_{tot \max}$, and if V_{CE} is then progressively increased, a sudden increase in the collector current will be noticed at some definite voltage, as shown in Fig.2. This is known as avalanche or first breakdown, and is caused by each charge carrier arriving at the depletion layer with sufficient energy, on average, to release one secondary carrier pair. This effect is cumulative and results in a self-sustaining discharge.

Avalanche breakdown is not usually a damaging phenomenon provided that the current (and thus the power dissipation) remains low.

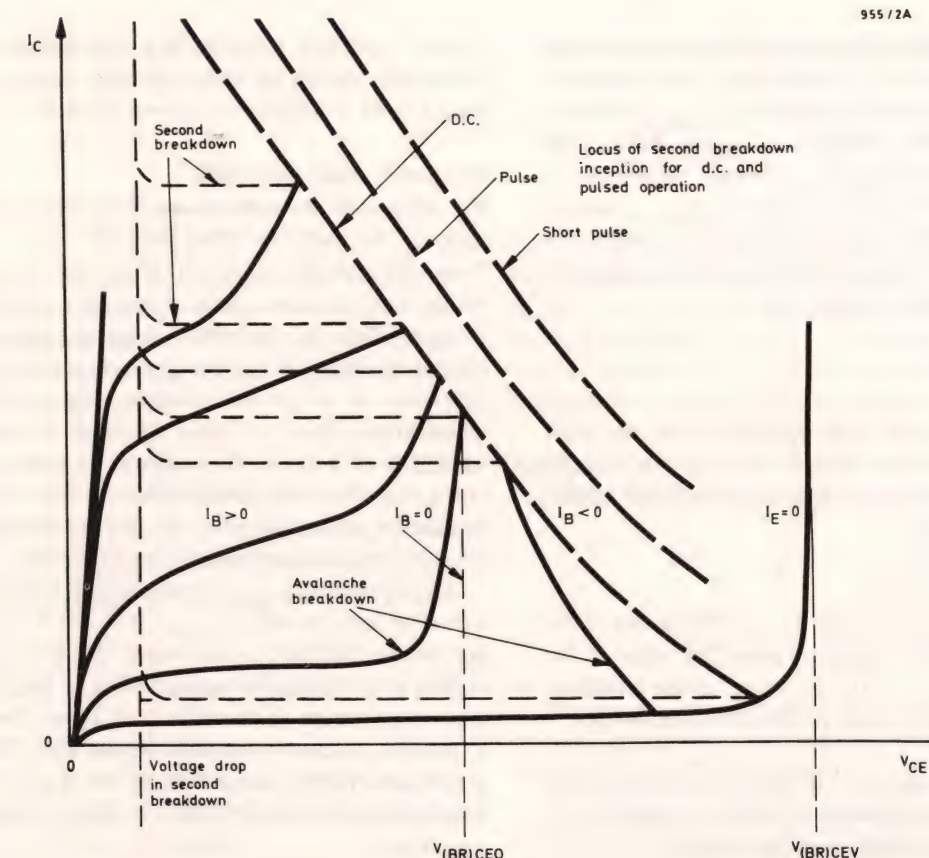


Fig.2 - A family of I_C/V_{CE} characteristics. Avalanche breakdown is portrayed by a sudden change in the characteristics, and second breakdown by an extremely rapid fall in voltage

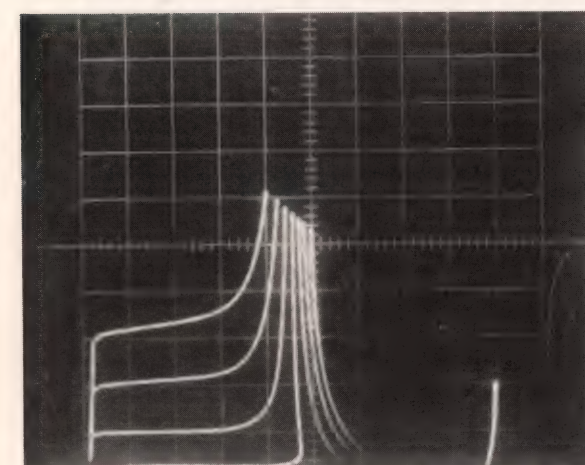


Fig.3 - First breakdown

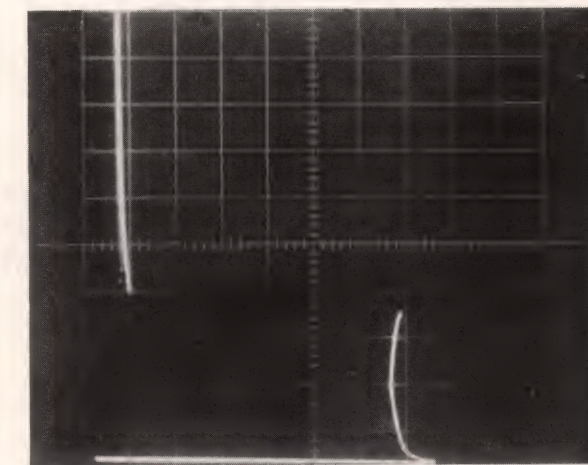


Fig.4 - Second breakdown; the actual breakdown curve is not visible owing to the high speed at which the second breakdown takes place (<100ns)

SECOND BREAKDOWN

If the collector current is allowed to increase without limit following avalanche breakdown, a second breakdown is observed. As shown in Fig.2, this is recognisable as a sudden reversal of the I_C/V_{CE} characteristic and usually damages the transistor. Second breakdown is caused by an area of high current density somewhere within the transistor chip. This high current density

causes a region of excessive temperature which can result in modification of the doping distribution, or even local melt-through of the junction. The graphical locus of second breakdown inception for pulsed operation moves towards higher collector dissipation values owing to the finite thermal capacity of transistors. Figs.3 and 4 show oscillograms of transistors entering avalanche and second breakdown.

There are two distinct types of breakdown mechanism which can lead to second breakdown. The maximum permissible collector-emitter voltage $V_{CE0\max}$ is chosen so that no avalanche breakdown occurs below this voltage. Thus, below $V_{CE0\max}$ second breakdown is thermally triggered. In contrast, above $V_{CE0\max}$ second breakdown is generally triggered entirely by avalanche, or first, breakdown. Second breakdown mechanisms are discussed in more detail in Appendix 2.

SOAR LIMITS

The four limits to the safe operating area are now explained, and the steps taken by the manufacturer to ensure that power transistors will operate reliably within these limits are set out.

The collector current limit

The maximum collector current $I_{C\max}$ forms one of the boundaries of the safe operating area. The value of the current limit depends on the structure of the transistor and is limited by one or more of the following factors:

- 1) power handling capability of the current feed system (for example, bonding wires or emitter metallisation);
- 2) dimensions of the emitter and base regions;
- 3) chip size.

Production quality is assured by tests carried out on regularly-obtained samples. These tests are designed to expose any deterioration in current-carrying capability. Devices are tested at or above the I_C rating for several thousand hours, and the results obtained are used to monitor life expectancy.

Transistors specifically designed for switching the current off in highly-inductive loads such as relays may have the collector current limit specified as a function of load inductance or load energy at particular values of base resistance and base-collector voltage.

The collector-emitter voltage limit

The maximum collector-emitter voltage $V_{CE0\max}$ forms another limit to the safe operating area. This limit should not normally be exceeded if second breakdown is to be avoided. The collector-emitter voltage limit is fixed by the design of the transistor and is determined by the dimensions and doping of the device structure. It is checked for all power transistors by programmable automatic test equipment during the manufacturing process.

The safe operating areas of transistors designed to be used in switching applications with an inductive load can have extended collector-emitter voltage limits. These extensions permit operation above $V_{CE0\max}$ for specified times under specified conditions of base-emitter

voltage, collector current, and emitter-base resistance. Great care should be taken if energy from an inductive load is to be dissipated in a power transistor.

The power dissipation limit

The maximum allowable power dissipation forms a third limit to the safe operating area of power transistors. Power dissipation causes a rise in junction temperature which will, in turn, start chemical and metallurgical changes. The rate at which these changes proceed is exponentially related to temperature, and thus prolonged operation of a power transistor above its junction temperature rating is liable to result in reduced life. Operation of a device at, or below, its power dissipation rating (together with careful consideration of the thermal resistances associated with the device) ensures that the junction temperature rating is not exceeded.

The value of $P_{tot\max}$ depends on the structure of the transistor and, as with $I_{C\max}$, it is checked by subjecting sample batches to prolonged dissipation or power cycling at, or about, the rating. Owing to the temperature-dependent nature of the effects of power dissipation, it is possible to devise accelerated test procedures which are suitable for the assessment of useful life. In addition, devices are tested under either, or both, of the following conditions:

- 1) at that combination of current and voltage where the $P_{tot\max}$ boundary intersects the second breakdown boundary;
- 2) at the maximum permitted V_{CE} for $I_{C\max}$.

During the manufacturing process, the thermal resistance of *all* power transistors is tested. This testing is performed at values of voltage and current corresponding to the boundary of the safe operating area. Thus the thermal resistance value quoted in our published data is a guaranteed maximum value since the thermal resistance falls as the operating point moves towards lower values of voltage and current.

Continuous power dissipation

The total power dissipation in a transistor P_{tot} may be calculated as follows:

$$P_{tot} = I_C V_{CE} + I_B V_{BE} \quad \dots (1)$$

The dissipation in the base can usually be disregarded, and so,

$$P_{tot} \approx I_C V_{CE} \quad \dots (2)$$

The heat dissipated in the collector-base junction flows through the thermal resistance between the junction and the mounting base $R_{th\ j-mb}$. The thermal

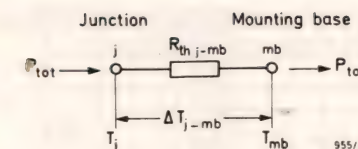


Fig. 5 — Heat transport in a transistor with power dissipation constant with respect to time

equivalent circuit of Fig. 5 illustrates this heat flow; P_{tot} can be regarded as a thermal current, and the temperature difference between the junction and mounting base ΔT_{j-mb} as a thermal voltage. By analogy with Ohm's law, it follows that:

$$P_{tot} = \frac{T_j - T_{mb}}{R_{th\ j-mb}} \quad \dots (3)$$

Fig. 6 shows the dependence of the maximum power dissipation on the temperature of the mounting base. $P_{tot\max}$ is limited either by the maximum temperature difference:

$$\Delta T_{j-mb\max} = T_{j\max} - T_{mb\ K} \quad \dots (4)$$

or by the maximum junction temperature $T_{j\max}$ ($T_{mb\ K}$ is the value of T_{mb} above which the maximum power dissipation must be reduced to maintain the operating point within the safe operating area).

In the first case, $T_{mb} \leq T_{mb\ K}$, and:

$$P_{tot\max\ K} = \frac{\Delta T_{j-mb\max}}{R_{th\ j-mb}} \quad \dots (5)$$

that is, the power dissipation has a fixed limit value ($P_{tot\max\ K}$ is the maximum d.c. power dissipation below $T_{mb\ K}$). If the transistor is subjected to a mounting-base temperature T_{mb1} , its junction temperature will be less than $T_{j\max}$ by an amount $(T_{mb\ K} - T_{mb1})$, as shown by the broken line in Fig. 6.

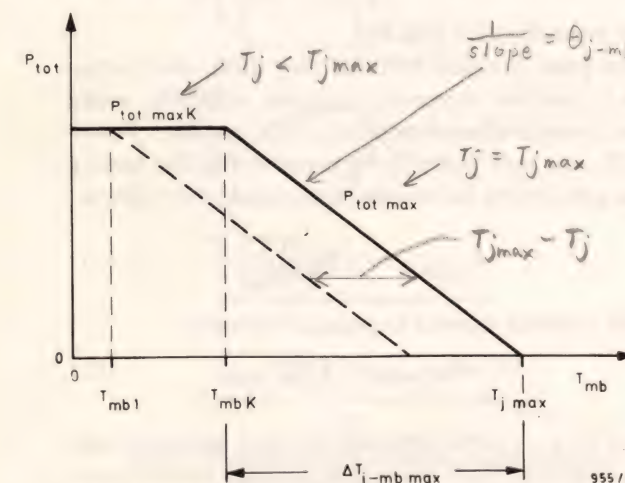


Fig. 6 — Maximum d.c. power dissipation in a transistor as a function of the mounting-base temperature

In the second case, $T_{mb} > T_{mb\ K}$, and:

$$P_{tot\max} = \frac{T_{j\max} - T_{mb}}{R_{th\ j-mb}} \quad \dots (6)$$

that is, the power dissipation must be reduced as the mounting-base temperature increases along the sloping straight line in Fig. 6. Eq. 6 shows that the lower the thermal resistance $R_{th\ j-mb}$, the steeper is the slope of the line. In this case, T_{mb} is the maximum mounting-base temperature than can occur in operation.

Example 1

The following data is provided for a particular transistor.

$$\begin{aligned} P_{tot\max\ K} &= 10\text{W} \\ T_{j\max} &= 125^\circ\text{C} \\ R_{th\ j-mb} &\leq 7^\circ\text{C/W} \end{aligned} \quad = ?$$

The maximum permissible power dissipation for continuous operation at a maximum mounting-base temperature of $T_{mb} = 80^\circ\text{C}$ is required.

Note that the maximum value of T_{mb} is chosen to be significantly higher than the maximum ambient temperature to prevent an excessively large heatsink being required.

From Eq. 6 we obtain:

$$\begin{aligned} P_{tot\max} &= \frac{125 - 80}{7} \text{ W} \\ &= 6.4\text{W} \end{aligned}$$

Provided that the transistor is operated within SOAR limits, this value is permissible since it is below $P_{tot\max\ K}$. The same result can be obtained graphically from the $P_{tot\max}$ diagram (Fig. 7) for the relevant transistor.

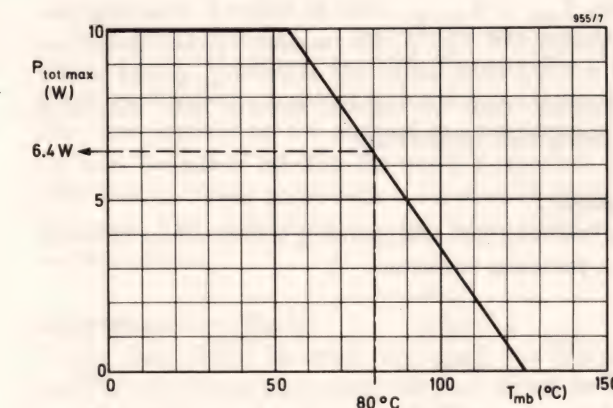


Fig. 7 — Example of the determination of the maximum power dissipation

Rectangular-pulse power dissipation

When a power transistor is subjected to a pulsed load, higher peak power dissipation is permitted. The materials in a power transistor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device.

This effect is given a fuller treatment later, but, in general, the shorter the pulse and the lower the frequency, the lower the temperature that the junction reaches. By analogy with Eq.3, it follows that:

$$P_{\text{tot M}} = \frac{T_j - T_{\text{mb}}}{Z_{\text{th j-mb}}}, \quad \dots (7)$$

where $Z_{\text{th j-mb}}$ is the transient thermal impedance between the junction and mounting base of the device. It depends on the pulse duration t_p , and the duty factor δ , where:

$$\delta = t_p / T, \quad \dots (8)$$

and T is the pulse period. Fig.8 shows a typical family of curves for thermal impedance against pulse duration, with duty factor as a parameter.

Again, the maximum pulse power dissipation is limited either by the maximum temperature difference $\Delta T_{\text{j-mb max}}$ (Eq.4), or by the maximum junction temperature $T_{\text{j max}}$, and so by analogy with Eqs.5 and 6.

$$P_{\text{tot M max K}} = \frac{\Delta T_{\text{j-mb max}}}{Z_{\text{th j-mb}}}, \quad \dots (9)$$

when $T_{\text{mb}} \leq T_{\text{mb K}}$, and:

$$P_{\text{tot M max}} = \frac{T_{\text{j max}} - T_{\text{mb}}}{Z_{\text{th j-mb}}}, \quad \dots (10)$$

when $T_{\text{mb}} > T_{\text{mb K}}$. That is, below a mounting-base temperature of $T_{\text{mb K}}$, the maximum power dissipation has a fixed limit value; and above $T_{\text{mb K}}$, the power dissipation must be reduced linearly with increasing mounting-base temperature.

Example 2

The following data and operating conditions are provided for a particular transistor.

$T_{\text{j max}} = 125^\circ\text{C}$	$T_{\text{mb}} = 75^\circ\text{C}$
$T_{\text{mb K}} = 55^\circ\text{C}$	$t_p = 0.1\text{ms}$
$Z_{\text{th j-mb}}$ as in Fig.8	$\delta = 0.2$

The maximum rectangular pulse power dissipation

is required. Fig.8 gives $Z_{\text{th j-mb}} = 2.5^\circ\text{C/W}$ and as $T_{\text{mb}} > T_{\text{mb K}}$, Eq.10 applies. Therefore:

$$P_{\text{tot M max}} = \frac{125 - 75}{2.5} = 20\text{W}.$$

Example 3

The above transistor is operated at the same power dissipation, but $t_p = 1\text{ms}$ and $\delta = 0.5$. The maximum mounting-base temperature is required.

Fig.8 gives $Z_{\text{th j-mb}} = 5.2^\circ\text{C/W}$, and rearranging Eq.10 gives:

$$T_{\text{mb}} = T_{\text{j max}} - P_{\text{tot M max}} \cdot Z_{\text{th j-mb}},$$

so that:

$$T_{\text{mb}} = (125 - 20 \times 5.2) = 21^\circ\text{C}.$$

However, this value is less than $T_{\text{mb K}}$ and consequently such operation is not permissible. The power dissipation must be reduced to below $P_{\text{tot M max K}}$; that is, from Eq.9:

$$P_{\text{tot M}} \leq \frac{125 - 55}{5.2} = 13.5\text{W}.$$

Alternatively, either t_p or δ (or both) must be reduced so that, using Eq.9, a thermal impedance of

$$Z_{\text{th j-mb}} \leq \frac{125 - 55}{20} = 3.5^\circ\text{C/W}$$

is obtained from Fig.8. Naturally, the other SOAR limits must also be observed.

The $Z_{\text{th j-mb}}$ values of Fig.8 are not only applicable to simple rectangular pulses; they can also be used with a continuous power dissipation superimposed, or with curves of any form, whether periodic or not. Fig.9 illustrates three important limit cases.

Short pulse duration (Fig.9a)

As the pulse duration becomes very short, the fluctuations of junction temperature become negligible, owing to the internal thermal capacity of the transistor. Consequently, the only factor to be considered is the heating of the junction by the average power dissipation; that is:

$$P_{\text{tot(av)}} = \delta P_{\text{tot M}}. \quad \dots (11)$$

The transient thermal impedance becomes:

$$\lim_{t_p \rightarrow 0} Z_{\text{th j-mb}} = \delta R_{\text{th j-mb}}. \quad \dots (12)$$

The $Z_{\text{th j-mb}}$ curves approach this value asymptotically as t_p decreases. Fig.8 shows that, for duty factors in the range 0.2 to 0.75, the limit values given by Eq.12 have virtually been reached at $t_p = 10^{-3}\text{ms}$.

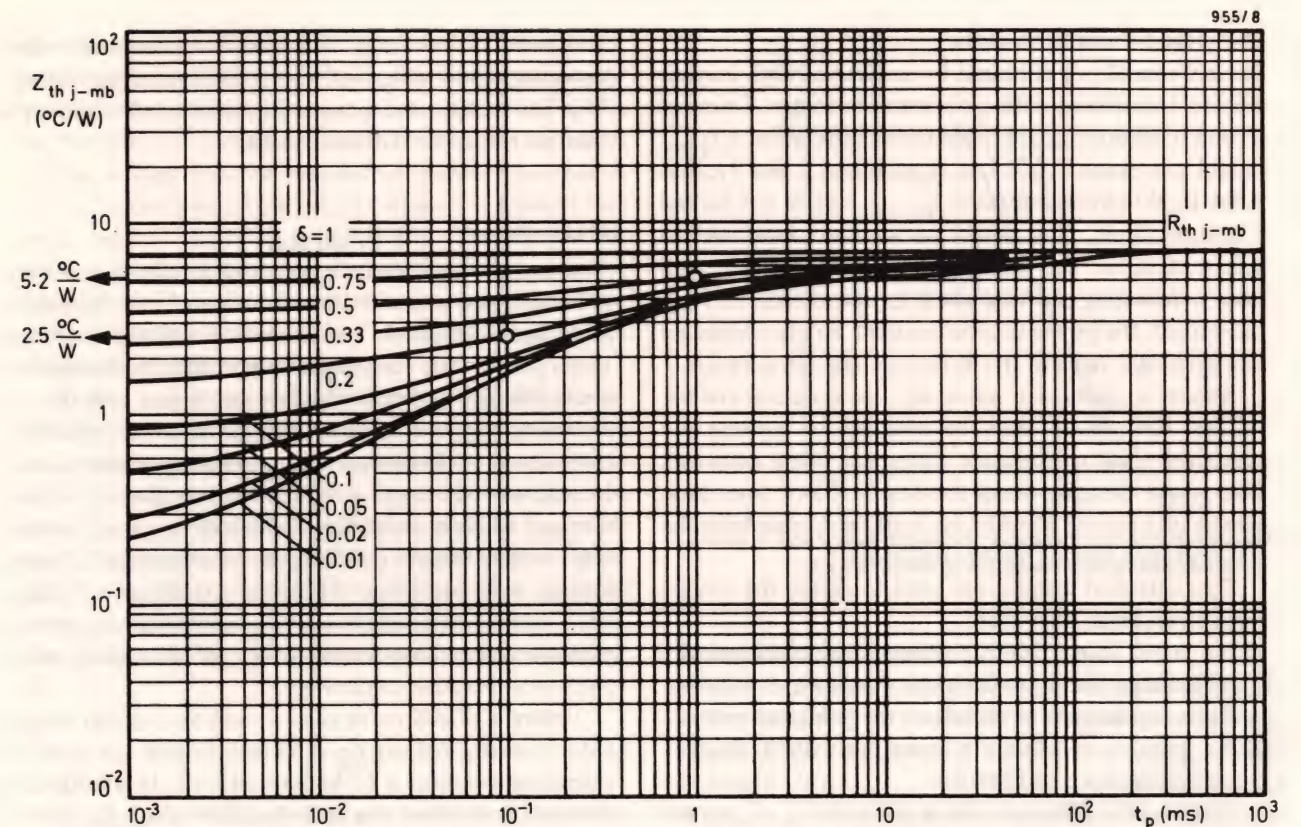


Fig.8 — Example of the presentation of the transient thermal impedance as a function of the pulse time with duty factor as parameter

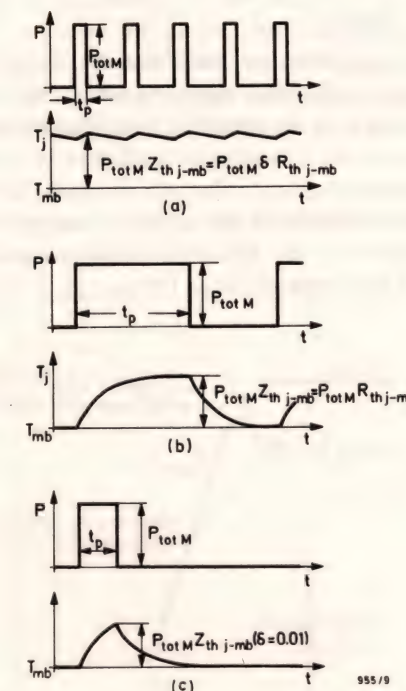


Fig.9 — Three limit cases of rectangular pulse loads:

- (a) short pulse duration
- (b) long pulse duration
- (c) single-shot pulse

Long pulse duration (Fig.9b)

As the pulse duration increases, the junction temperature approaches a stationary value towards the end of a pulse. The transient thermal impedance tends to the thermal resistance for continuous power dissipation; that is:

$$\lim_{t_p \rightarrow \infty} Z_{\text{th j-mb}} = R_{\text{th j-mb}}. \quad \dots (13)$$

Fig.8 shows that $Z_{\text{th j-mb}}$ approaches this value as t_p becomes large. In general, transient thermal effects die out in most power transistors within 0.1 to 1.0 seconds. This time depends on the material and construction of the case, the size of the chip, the way it is mounted, and other factors. Power pulses with a duration in excess of this time have approximately the same effect as a continuous load.

Single-shot pulses (Fig.9c)

As the duty factor becomes very small, the junction tends to cool down completely between pulses so that each pulse can be treated individually. When considering single pulses, the $Z_{\text{th j-mb}}$ values for $\delta = 0.01$ (Fig.8) give sufficiently accurate results.

The second breakdown limit

Second breakdown is caused by an area of high current density somewhere within the transistor chip. To avoid second breakdown, local temperature differences ΔT_{j-mb} should not exceed 16°C (see Appendices 2 and 3); that is, the local thermal resistance $r_{th j-mb}$ should not exceed a certain limit. The onset of second breakdown is independent of the mounting-base temperature since local overheating can take place independently of T_{mb} . In contrast, the power dissipation limit is only applicable to a particular value of the mounting-base temperature.

Above a particular value of the collector-emitter voltage, the power must be reduced to prevent the maximum local temperature difference being exceeded. This power derating forms the fourth SOAR boundary, namely the second breakdown limit, and completes the safe operating area of power transistors.

Two different criteria are used to define the second breakdown limit. They are:

- 1) the limit above which excessive local temperature differences occur in the chip, causing the apparent thermal resistance to rise above the published value;
- 2) the limit above which the transistor will be damaged during its expected life time.

The second definition takes no account of thermal effects within the chip, and in fact allows some degree of local overheating. The first definition is more stringent and thus offers a higher degree of protection against second breakdown. Consequently we use the first definition for the vast majority of SOAR data.

Fig.10 shows how second breakdown is defined according to this criterion. The local thermal resistance $r_{th j-mb}$ is that thermal resistance arising from the highest local temperature difference within the chip, and $r_{th j-mb}$ becomes greater than the published value of the thermal resistance $R_{th j-mb}$ when a hot spot begins to form within the chip.

At voltage and current values well below the SOAR boundary, the thermal resistance is significantly lower than the published value.

Note that the junction temperature falls as the opera-

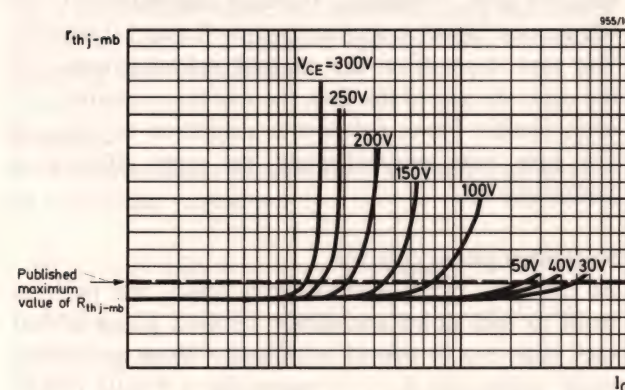


Fig.10 - Definition of the second breakdown limit

tion point moves along the second breakdown boundary towards higher values of the collector-emitter voltage. This is because the power dissipation falls while the thermal resistance remains constant.

SOAR FOR $V_{CE} < V_{CE0 \max}$

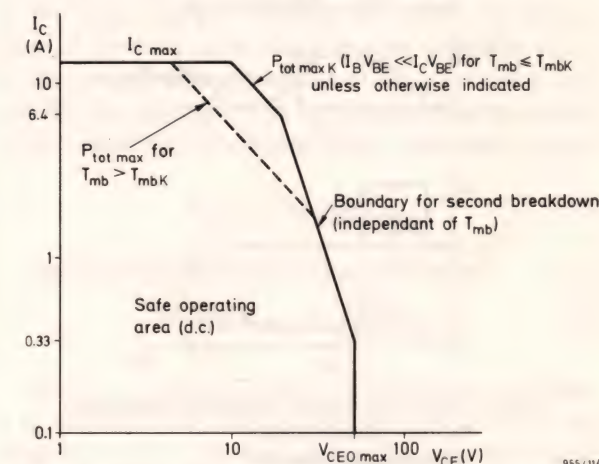
The boundaries of the safe operating area have now been defined and the methods used to specify the boundary conditions described. For a power transistor operating under steady-state conditions, each of the four boundaries should be regarded as an absolute maximum, even though exceeding any one of them may not result in immediate destruction of the device. Driving a transistor into second breakdown will result in sudden destruction, or at least damage, whereas exceeding the power or current ratings will usually cause chemical or metallurgical changes leading to reduced life. Thus, the SOAR curve defines that region of possible I_C/V_{CE} combinations within which a transistor operating point should remain under the worst probable conditions.

Before a SOAR curve can be used as a circuit design aid it usually has to be modified to suit the type of operating conditions to be experienced. In addition, a derating procedure can and should be used for power transistors in all applications. The circuit designer is then able to ensure a reasonable compromise between power device cost and component tolerance, whilst arriving at a sound reliable design.

The d.c. SOAR

The safe operating area valid for d.c. conditions forms the basis for all other operating areas. Fig.11 shows an example of such an operating area. The individual limits which form the operating area will now be considered in more detail.

For small values of the collector current, the vertical line is given by the maximum collector-emitter voltage with the base open-circuited ($V_{CE0 \max}$). This prevents

Fig.11 - D.C. operating area of a transistor for $V_{CE} < V_{CE0 \max}$

operation of the transistor in the area where avalanche breakdown can occur (see Fig.2). This limit applies only up to a certain collector current (about 0.33A in Fig.11). As the collector current increases further, the collector-emitter voltage must be reduced to prevent the onset of second breakdown. This fall in voltage is a straight line (with negative slope) on a log-log grid. The value of this slope is greater than unity; that is, the collector power dissipation ($I_C V_{CE}$) increases with decreasing collector-emitter voltage. This boundary is independent of the temperature of the mounting base.

As the collector current increases along the second breakdown boundary, a point may be reached where the maximum power dissipation is reached (at $I_C = 6.4\text{A}$ in Fig.11). As I_C increases further, V_{CE} must be reduced to keep $P_{tot \max}$ constant, that is the product $I_C V_{CE}$ must be kept constant; the slope of this boundary on a log-log grid is therefore -1 . We have assumed that the base power dissipation ($I_B V_{BE}$) can be disregarded. If not, the product $I_C V_{CE}$ must be reduced correspondingly; that is:

$$I_C V_{CE} = P_{tot \max} - I_B V_{BE} \quad \dots (14)$$

$P_{tot \max}$ is calculated from Eq.5 or 6, but the boundary is usually plotted for $P_{tot \max} K$; that is, it applies to mounting-base temperatures below $T_{mb K}$.

As the mounting-base temperature increases, the power dissipation boundary meets the second breakdown limit at progressively lower values of I_C , and can eventually exclude the second breakdown limit completely (Fig.12). Alternatively, the situation can be reversed if the maximum power dissipation is very high, or the mounting-base temperature is relatively low (Fig.13).

For small values of the collector-emitter voltage, the safe operating area is limited by the maximum collector current (horizontal line in Fig.11).

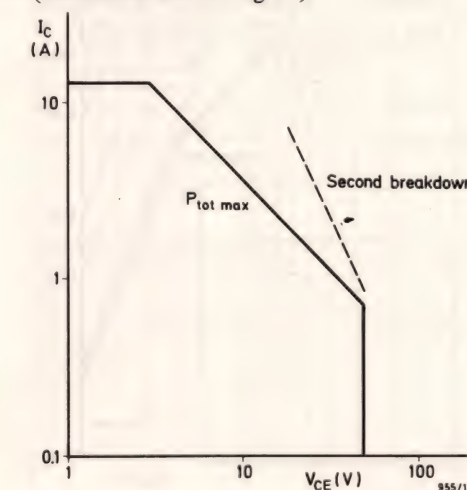


Fig.12 - The second breakdown boundary can be excluded when the maximum power dissipation is relatively low

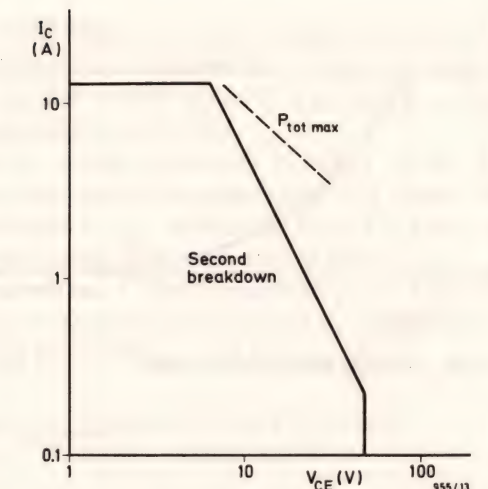


Fig.13 - The power dissipation boundary can be excluded when the maximum power dissipation is relatively high

Intermittent operation

All the limits that are either wholly or partly thermally determined may be extended for intermittent operation. These limits are second breakdown, $I_{C \max}$ which becomes $I_{CM \max}$, and $P_{tot \max}$ which becomes $P_{tot M \max}$. Note that although second breakdown is generally thermally triggered when $V_{CE} < V_{CE0 \max}$, its onset does not depend on the temperature of the mounting base. Thus the second breakdown limit can be extended for intermittent operation but, in contrast to the power dissipation limit, it is not applicable to a particular value of T_{mb} . The actual extensions of these ratings will depend on the duration of the operation period (that is, pulse duration) and the frequency with which operation occurs (that is, duty factor).

If power is applied to a transistor, the device will immediately commence to warm up (Fig.14). If the power dissipation continues, a balance will be struck between heat generation and removal resulting in the stabilisation of T_j and ΔT_{j-mb} . Some heat energy will be stored by the thermal capacity of the device, and the stable conditions will be determined by the thermal resistances associated with the transistor and its thermal environment. When the power dissipation ceases, the

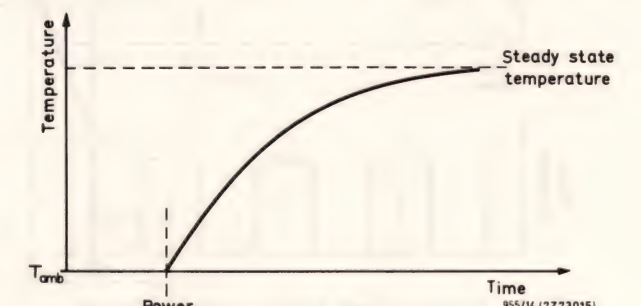


Fig.14 - Heating of a transistor chip

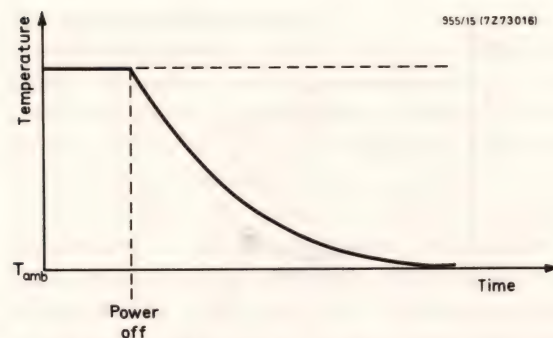


Fig. 15 — Cooling follow the same law

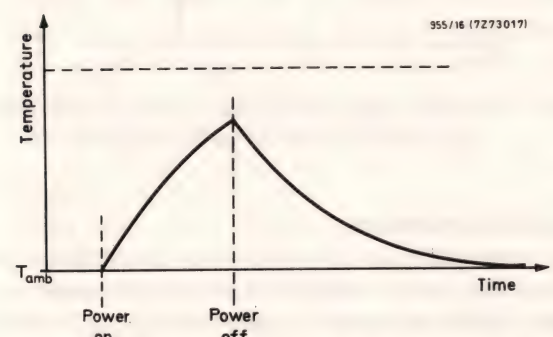


Fig. 16 — The peak temperature caused by a short power pulse can be less than the steady-state temperature resulting from the same power

device will cool (the heating and cooling laws will be identical, see Fig. 15). However, if the power dissipation ceases before the temperature of the transistor stabilises, the peak values of T_j and ΔT_{j-mb} will be less than the values reached for the same level of continuous power dissipation (Fig. 16). If the second pulse is identical to the first, the peak temperature attained by the device at the end of the second pulse will be greater than that at the end of the first pulse. Further pulses will build up the temperature, until some new stable situation is attained (Fig. 17). The temperature of the device in this

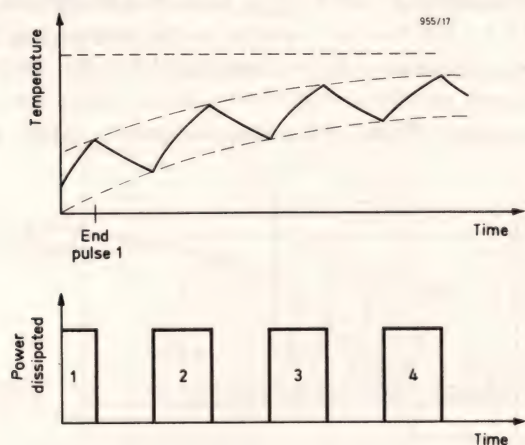
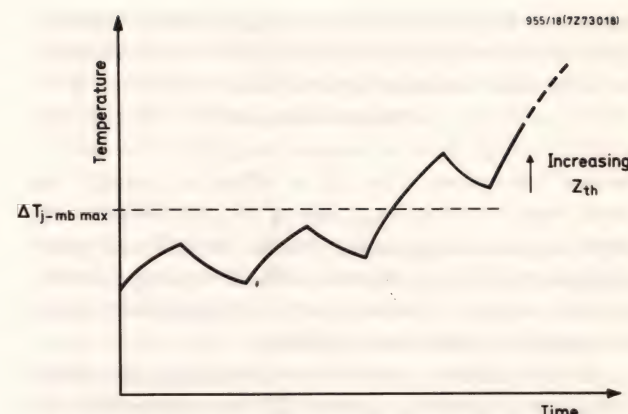
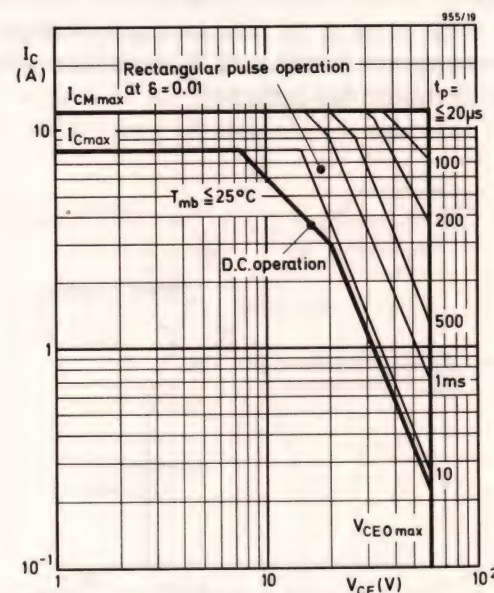


Fig. 17 — A train of power pulses increases the average temperature if the device does not have time to cool between pulses

Fig. 18 — If any pulse causes $\Delta T_{j-mb \max}$ to be exceeded, current concentration will result and the effect is cumulative

stable condition will fluctuate above and below the mean. If the upward excursions extend into the region of either excessive T_j or ΔT_{j-mb} , then either the life expectancy of the device will be reduced, or current concentration will occur, possibly leading to second breakdown and destruction (Fig. 18). This can happen with high-power low-duty-factor pulses, even though the *average* power is below the d.c. rating of the device.

Fig. 19 shows a typical safe operating area for d.c. operation of a low-voltage power transistor. The corresponding rectangular-pulse operating areas with a fixed duty factor, $\delta = 0.01$, and the pulse time t_p as a parameter, are also shown. For very small values of the duty factor, periodic pulses virtually operate as single-shot pulses so that these boundaries represent the largest possible extension of the operating area for particular pulse times. When the pulse time becomes very short,

Fig. 19 — D.C. and rectangular pulse operating areas with fixed parameters δ , t_p , and T_{mb}

neither the power dissipation nor the second breakdown has a limiting action and $I_{CM \max}$ and $V_{CE0 \max}$ form the only limits. This rectangle represents the largest possible pulse operating area.

SOAR for intermittent operation at random values of δ and t_p

Most published data contains further information which can be used to calculate SOAR limits for any values of δ and t_p .

The maximum power dissipation is obtained from Eqs. 9 or 10 and a corresponding operating area boundary, parallel to the d.c. boundary, obtained (the transient thermal impedance is given in the form of graphs such as Fig. 8). An alternative approach can be used to check that the permissible power dissipation limits are complied with. Eqs. 9 and 10 should be used to ensure that $\Delta T_{j-mb \max}$ and $T_{j \max}$ are not being exceeded. If both are being exceeded (or $\Delta T_{j-mb \max}$ only), the value of $P_{tot M}$, t_p , or δ should be reduced appropriately. If only $T_{j \max}$ is being exceeded, the mounting-base temperature can be reduced by introducing better cooling instead. The heatsink required for this purpose can generally be designed according to the average power dissipation, which for rectangular pulses is given by Eq. 11:

$$P_{tot(av)} = \delta P_{tot M}$$

A discussion of heatsinks and their design is given later in this article.

The second breakdown limits for pulsed operation are more complicated to calculate since, in general, they do not run parallel to each other. It is preferable to form them graphically, as in Fig. 20.

First, the second breakdown boundary of the d.c. operating area should be extended until it crosses the horizontal limit $I_{C \max}$ at point S. Point T is where the second breakdown limit and vertical limit $V_{CE0 \max}$ cross. Points S' and T', which enable the pulsed operation boundaries to be drawn, are obtained by employing two multiplying factors, $M_{SB(I)}$ and $M_{SB(V)}$ where:

$$M_{SB(V)} = \text{voltage multiplying factor, and} \\ M_{SB(I)} = \text{current multiplying factor.}$$

Now,

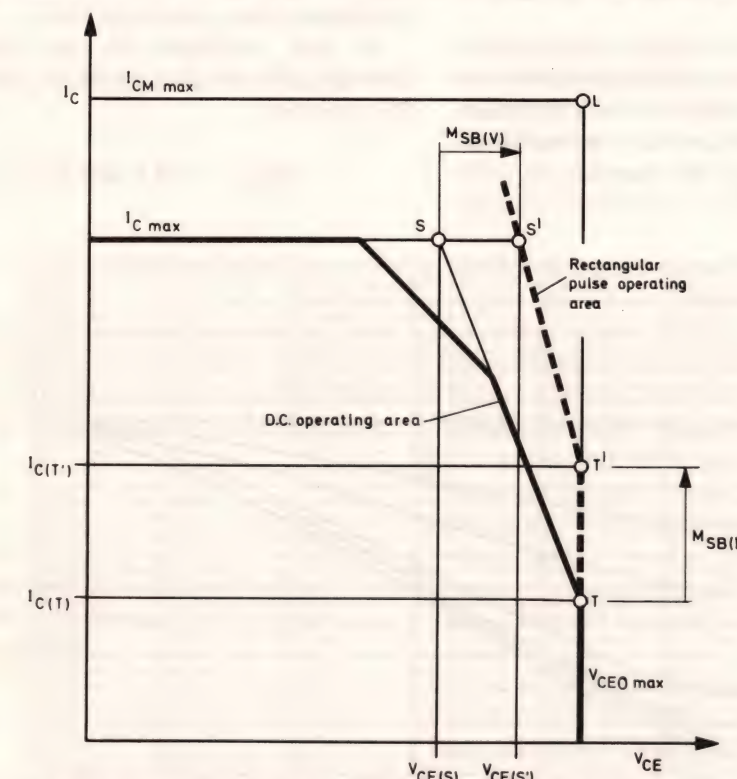
$$V_{CE(S')} = M_{SB(V)} V_{CE(S)}, \quad \dots (15)$$

provided that $V_{CE(S')} \leq V_{CE0 \max}$; and

$$I_{C(T')} = M_{SB(I)} I_{C(T)}, \quad \dots (16)$$

provided that $I_{C(T')} \leq I_{CM \max}$. The voltage $V_{CE(S')}$ is the value of V_{CE} at the point S', and so on.

Fig. 21 shows how $M_{SB(V)}$ and $M_{SB(I)}$ are presented in the published data. Note that the boundaries formed by $I_{CM \max}$ and $V_{CE0 \max}$ should not be exceeded and thus the boundary S' - T' should not move outside the rectangle formed by the axes and point L (Fig. 20), even

Fig. 20 — Construction of the second breakdown boundary for rectangular pulse operation with the aid of the multiplying factors $M_{SB(V)}$ and $M_{SB(I)}$

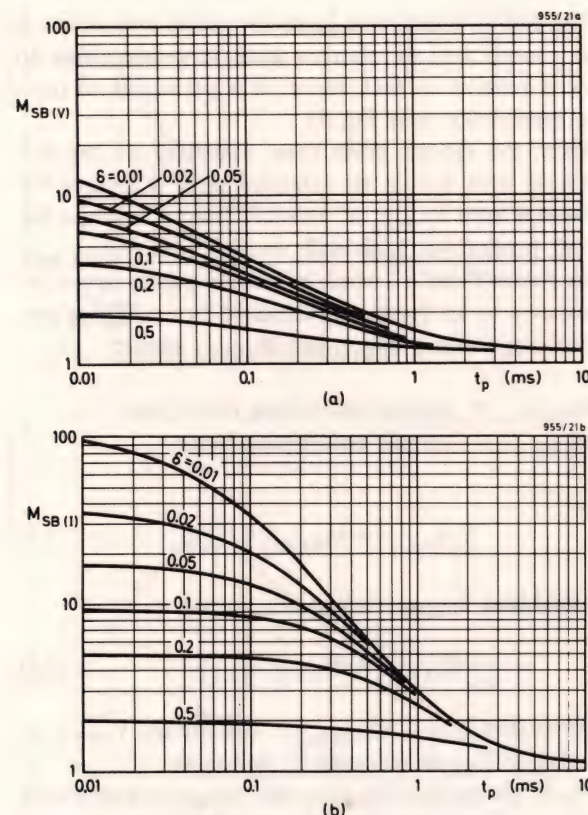


Fig. 21 - Second breakdown multiplying factors as a function of pulse time, with duty factor as a parameter

if the multiplying factors are so large as to indicate that it should do so.

Again, the second breakdown boundary is independent of the mounting-base temperature. The power dissipation boundary, however, is only applicable to a particular mounting-base temperature. It can only be moved to higher values of I_C and V_{CE} by lowering T_{mb} , if $T_{mb} > T_{mbK}$.

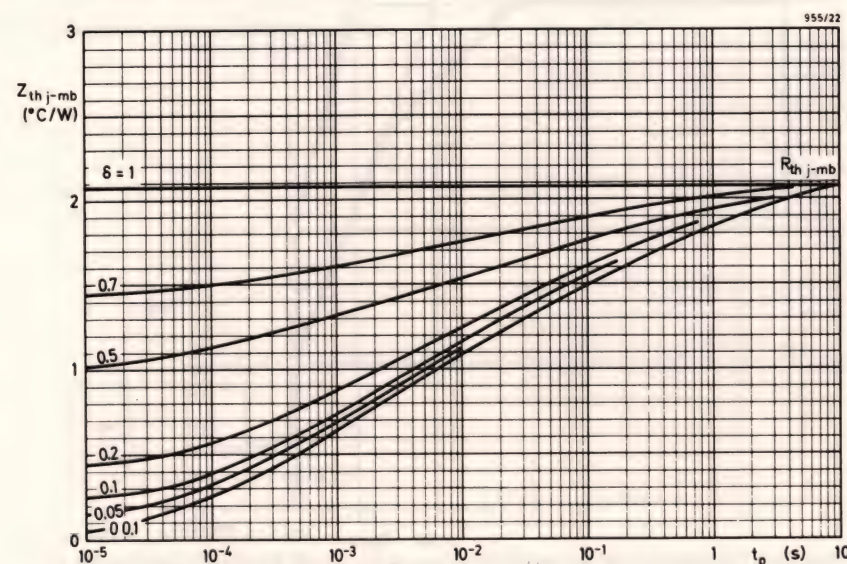


Fig. 22 - Transient thermal impedance for Example 4

Example 4

In addition to Figs. 19, 21a, 21b, and 22, the following data is provided for a particular transistor.

$$T_{j \max} = 150^\circ\text{C}$$

$$T_{mbK} = 25^\circ\text{C}$$

$$I_{CM \max} = 12\text{A}$$

The transistor is to be operated by a periodic squarewave with:

$$t_p = 0.2\text{ms}, \delta = 0.1.$$

The maximum occurring mounting-base temperature $T_{mb} = 80^\circ\text{C}$. The relevant pulse SOAR is required.

This is obtained as follows.

1) Draw the d.c. operating area (see Fig. 23). Plot the new collector current boundary ($I_{CM \max} = 12\text{A}$), and then calculate the new power dissipation limits.

For the given values of t_p and δ , Fig. 22 shows that $Z_{th j-mb} = 0.5^\circ\text{C/W}$. Eq. 10 gives:

$$P_{tot M \max} = \frac{150 - 80}{0.5} = 140\text{W}.$$

2) Construct the $P_{tot M \max}$ limit. Assuming that the base power dissipation is negligible, $V_{CE}I_C = 140\text{W}$. Calculate the co-ordinates of a point such as P_1 ($I_C = 7\text{A}$, $V_{CE} = 20\text{V}$) and draw a line through P_1 parallel to the continuous power dissipation limit.

3) Now determine the new second breakdown boundary. For the given values of t_p and δ , Figs. 21a and 21b show that:

$$M_{SB(V)} = 2.4, \text{ and } M_{SB(I)} = 7.3.$$

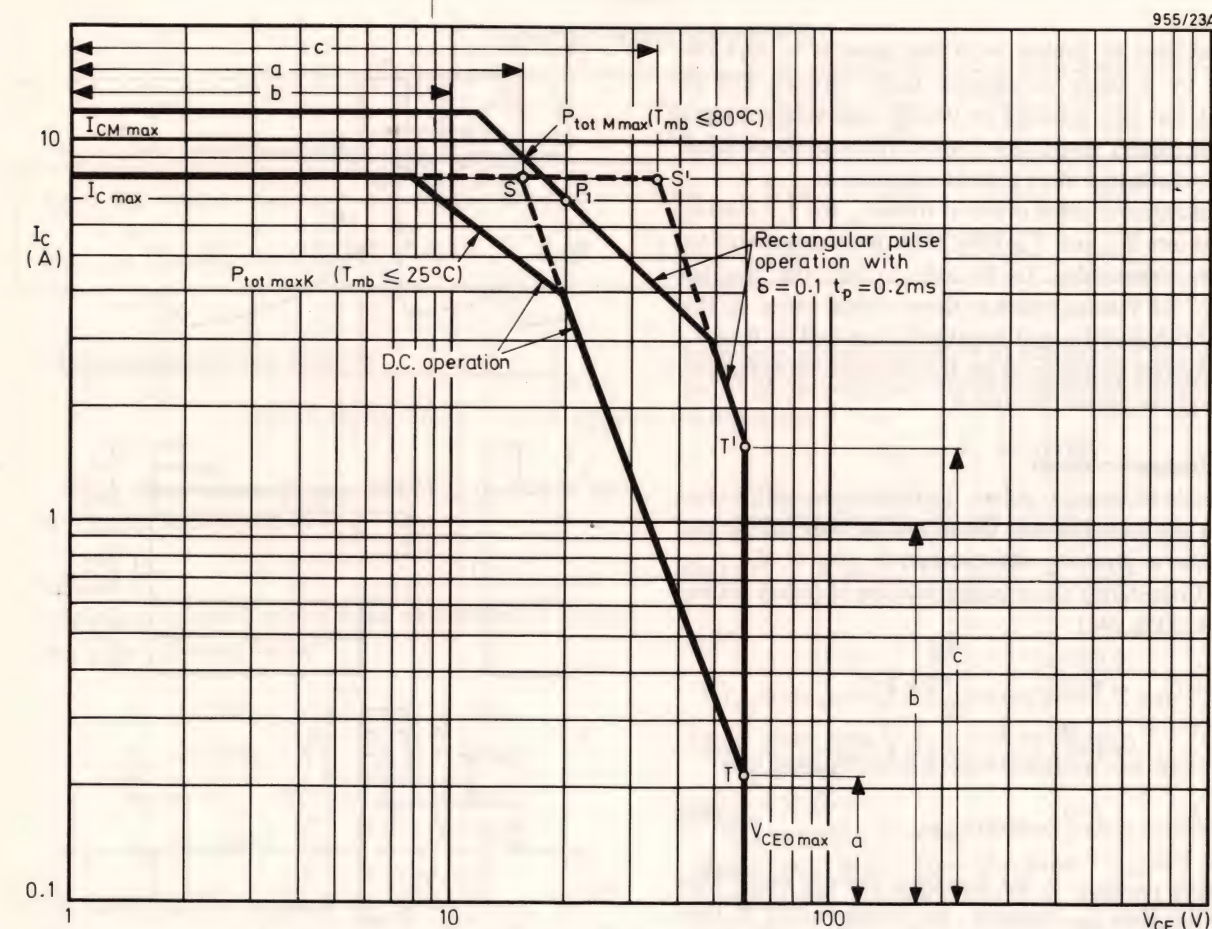


Fig. 23 - Construction of the pulse operating area for Example 4

Now, $V_{CE(S)} = 13\text{V}$, and $I_{C(T)} = 0.22\text{A}$ (Fig. 23), and Eqs. 15 and 16 give:

$$V_{CE(S')} = (2.4 \times 13)\text{V} = 31\text{V},$$

and:

$$I_{C(T')} = (7.3 \times 0.22)\text{A} = 1.6\text{A}.$$

The new second breakdown boundary can now be drawn.

4) An alternative method of obtaining the co-ordinates of S' and T' is to take advantage of the logarithmic nature of the two axes. Eqs. 15 and 16 can be rewritten:

$$c = a + b \log M_{SB}, \quad \dots (17)$$

where c , a , and b are the appropriate distances in Fig. 23; c and a can be measured (in a positive direction) from any factor-of-ten point on the axis. For the construction of the point T' , for example:

$$c = 16.6\text{mm} + 50.3\text{mm} \log 7.3 = 60.0\text{mm}.$$

The safe operating area for an intermittent load, with specified values of the pulse duration and duty factor,

has now been defined. The power dissipation limit is only applicable to a mounting-base temperature of 80°C . The other limits remain unaffected by the value of T_{mb} , unless they are curtailed by the movement of the power dissipation limit which results from an increase in T_{mb} .

SOAR for composite waveforms

In practice, a power transistor frequently has to handle composite waveforms, rather than the simple rectangular pulses that have been considered so far. Composite waveforms occur in switching applications, for instance, where low power dissipation occurs during the on and off states, but high power peaks occur during the switching between states. This type of signal can be simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of t_p and δ . The safe operating area for each pulse can then be found.

As an example, consider Fig. 24a, where the power dissipation of a switching waveform has been converted into equivalent rectangular pulses P_x and P_y . The power P_o is the dissipation with the transistor switched on, the dissipation with the device switched off being negligible. A

rough method of dealing with this signal is to approximate it by a single rectangular pulse (broken line in Fig.24a), but this provides an unduly high safety margin when calculating dissipation limits. The superimposition method results in a more precise calculation.

The maximum loads occur at times t_x and t_y , causing temperatures T_{jx} and T_{jy} (Fig.24b). Both cases must be examined separately. To be able to add the thermal effects of the various pulses at these critical times, all the pulses (both positive and negative) must end at time t_x or t_y . Positive pulses increase the junction temperature, while negative pulses decrease it.

Power dissipation limits

With simple rectangular pulses, the temperature difference between the junction and the mounting base at the end of a pulse is given by the product $P_{tot} M \times Z_{th j-mb}$ (Eq.7). Considering the superimposition of pulses ending at time t_x (Fig.24c):

$$T_{jx} - T_{mb} = P_x Z_{th j-mb}(t_{px}) + P_y Z_{th j-mb}(t_{py}) + P_o Z_{th j-mb}(t_{po}) - P_y Z_{th j-mb}(t_{p3}) - P_o Z_{th j-mb}(t_{p1}), \quad \dots (18a)$$

where $Z_{th j-mb}(t_p)$ is the transient thermal impedance for a pulse time t_p . Similarly, for pulses ending at time t_y (Fig.24d):

$$T_{jy} - T_{mb} = P_y Z_{th j-mb}(t_{py}) + P_o Z_{th j-mb}(t_{p4}) + P_x Z_{th j-mb}(t_{p5}) - P_o Z_{th j-mb}(t_{py}) - P_x Z_{th j-mb}(t_{p6}), \quad \dots (18b)$$

These equations now replace Eq.7 when pulses of this nature are considered. As with Eqs.9 and 10, they can now be used to determine (without a SOAR diagram having to be drawn) whether $T_{j \max}$ and $\Delta T_{j-mb \max}$ (or $\Delta T_{j-mb \max}$ only) are being exceeded, in which case the pulse values should be reduced. Alternatively, if only $T_{j \max}$ is being exceeded, the mounting-base temperature can be reduced.

To calculate T_{mb} , or to design a heatsink, the average power dissipation is required and in this case is given by:

$$P_{tot(av)} = \frac{P_x t_{px} + P_o t_{po} + P_y t_{py}}{T} \quad \dots (19)$$

Second breakdown limits

As before, the second breakdown boundary is best formed graphically; that is, by shifting the original boundary with the use of multiplying factors.

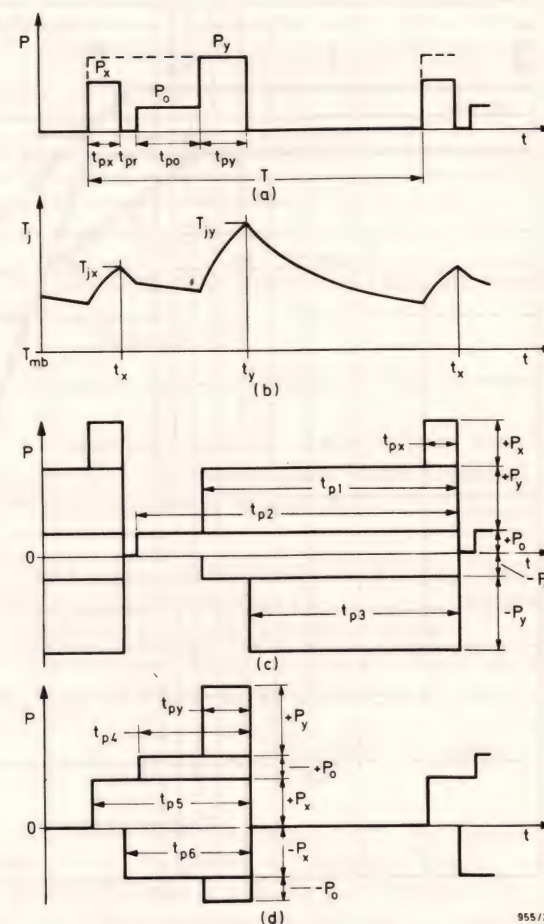


Fig.24 — Example of a rectangular composite power dissipation: (a) power dissipation variation by equivalent rectangular pulses; (b) junction temperature variation; (c) and (d) simulation of the power dissipation variation by the superimposition of periodic series of similar rectangular pulses

In a switching transistor, low power dissipation occurs during the on state (P_o , Fig.24); that is, it operates at a low collector-emitter voltage and thus far removed from the second breakdown boundary. Therefore, the power per unit volume is relatively small so that the chip does not suffer any overheating. Consequently, the power dissipation P_o hardly contributes to the second breakdown, and to take it into account when calculating the multiplying factors would result in excessive safety margins. Therefore, the following procedure is more practical. Form an equivalent power pulse with an amplitude P'_M equal to the maximum peak value of the power dissipation (P_y in this case). The energy of the pulse should be specified in such a way that the average value of the power dissipation agrees with the value calculated from Eq.19. The duration of this equivalent is then given by:

$$t'_p = \frac{P_{tot(av)} T}{P'_M}, \quad \dots (20a)$$

TABLE 1
Numerical Values (Example 5)

(μs)	t_{px} 10	t_{p1} 48	t_{p2} 198	t_{p3} 28	t_{py} 20	t_{p4} 170	t_{p5} 182	t_{p6} 172
$\delta (=t_p/T)$	0.05	0.24	0.99	0.14	0.10	0.85	0.91	0.86
$Z_{th j-mb}$ (Fig.22) ($^{\circ}C/W$)	0.17	0.60	2.08	0.40	0.27	1.8	1.9	1.9

and the equivalent duty factor is:

$$\delta' = t'_p/T. \quad \dots (20b)$$

Using these values, $M_{SB(I)}$ and $M_{SB(V)}$ can be read from graphs such as Fig.21.

Example 5

A transistor is loaded with a signal such as that in Fig.24a having the following values:

$$\begin{aligned} P_x &= 25W & t_{px} &= 10\mu s \\ P_y &= 100W & t_{py} &= 20\mu s \\ P_o &= 5W & t_{pr} &= 2\mu s \\ t_{po} &= 150\mu s & T &= 200\mu s \end{aligned}$$

The following information is also given: $T_{j \max} = 150^{\circ}C$, $\Delta T_{j-mb \max} = 125^{\circ}C$, $R_{th j-mb} = 2.1^{\circ}C/W$, and the families of curves shown in Figs.19, 21a, 21b, and 22 are applicable. The power dissipation and second breakdown boundaries are required.

Fig.22 gives values of $Z_{th j-mb}$ for each partial rectangular pulse; these values are compiled in Table 1. The t_p values not given above can be calculated by referring to Fig.24.

Using Eqs.18, ΔT_{j-mb} can be calculated for times t_x and t_y :

$$T_{jx} - T_{mb} = 32^{\circ}C, \quad T_{jy} - T_{mb} = 35^{\circ}C.$$

ΔT_{j-mb} does not exceed $\Delta T_{j-mb \max}$ in either case, and so the specified pulse values do not need to be reduced. However, adequate cooling must be provided to ensure that the junction temperature never exceeds $T_{j \max}$. The junction will reach its peak temperature at time t_y (Fig.24b), when the maximum mounting-base temperature is therefore:

$$\begin{aligned} T_{mb} &= T_{j \max} - \Delta T_{j-mb}, \\ &= (150 - 35)^{\circ}C, \\ &= 115^{\circ}C. \end{aligned}$$

To obtain the second breakdown boundary, follow the procedure outlined above; that is, consider an

equivalent power pulse with an amplitude P'_M equivalent to the maximum peak value of the power dissipation (P_y in this case):

$$P'_M = P_y = 100W.$$

Using Eqs.20a and 20b, we obtain:

$$t'_p = \frac{15 \times 200}{100} = 30\mu s,$$

and:

$$\delta' = \frac{30}{200} = 0.15.$$

Fig.21, then gives $M_{SB(V)} = 4$ and $M_{SB(I)} = 1.2$.

The second breakdown boundary can now be constructed as above.

The switching times of modern power transistors are usually very short. Thus the times t_{px} and t_{py} , and therefore the corresponding duty factors, tend to be small with respect to the thermal time-constants of the transistor. Consequently, relatively small values for the multiplying factors $M_{SB(V)}$ and $M_{SB(I)}$ are obtained. As a result, the power dissipation and second breakdown boundaries frequently lie outside the rectangle formed by $I_{CM \max}$ and $V_{CEO \max}$, in which case this rectangle constitutes the safe operating area.

SOAR for non-periodic waveforms

The simplest example of a non-periodic load is a single-shot rectangular pulse (Fig.25). In this case, the transient thermal impedance at a duty factor of $\delta = 0.01$ can be used as a basis for calculating the power dissipation limit. Thus:

$$T_j - T_{mb} = P_M Z_{th j-mb}(t_p)_o, \quad \dots (21)$$

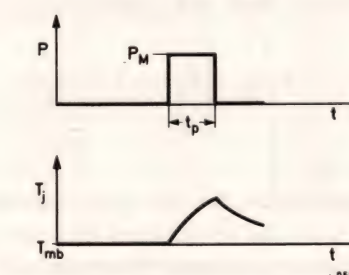


Fig.25 — Single-shot rectangular pulse

where $Z_{th j-mb}(t_p)_o$ is the transient thermal impedance for a pulse time t_p and with $\delta = 0.01$. Also, the second breakdown boundary can be calculated using Eqs.15 and 16, and the multiplying factors appropriate to $\delta = 0.01$.

When dealing with a series of similar pulses that occur only once or at long intervals (Fig.26), the superimposition method outlined above can be used. The transient thermal impedance and multiplying factors are read from the relevant family of curves for $\delta = 0.01$. For the example shown in Fig.26, the temperature difference at the end of the third pulse is given by:

$$T_j - T_{mb} = P_M \left\{ Z_{th j-mb}(t_{px})_o + Z_{th j-mb}(t_{p1})_o + \right. \\ \left. + Z_{th j-mb}(t_{p2})_o - Z_{th j-mb}(t_{p4})_o - \right. \\ \left. - Z_{th j-mb}(t_{p3})_o \right\} \dots (22)$$

The relevant multiplying factors are given by:

$$\frac{1}{M_{SB}} = \frac{1}{M_{SB_o}(t_{px})} + \frac{1}{M_{SB_o}(t_{p1})} + \frac{1}{M_{SB_o}(t_{p2})} - \\ - \frac{1}{M_{SB_o}(t_{p3})} - \frac{1}{M_{SB_o}(t_{p4})} \dots (23)$$

This equation applies to both $M_{SB(V)}$ and $M_{SB(I)}$; the index o indicating that the value of M_{SB} at $\delta = 0.01$ is required.

A group of composite rectangular pulses that occurs only once or very rarely can be dealt with by weighting the individual terms in Eq.22 with the relevant power amplitudes as in Eqs.18a and 18b. For example, the power load represented by Fig.27 can be simulated by Fig.24d, and the maximum junction temperature at the end of time t_{py} can be calculated using Eq.18b (remembering that all the $Z_{th j-mb}$ values are at $\delta = 0.01$).

To obtain the multiplying factors, the procedure outlined previously should be repeated. The power variation is approximated by an equivalent pulse which has the highest occurring amplitude (P_y in this case) and equal total energy. Thus, the equivalent pulse duration is given by:

$$t'_p = \frac{P_x t_{px} + P_o t_{po} + P_y t_{py}}{P_y} \dots (24)$$

The multiplying factors for this pulse time and a duty factor of $\delta = 0.01$ can be obtained from the published data. The second breakdown boundary can then be constructed.

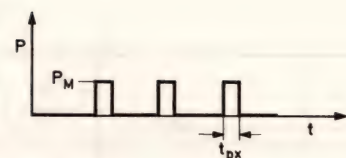


Fig.26 - Once-only series of similar rectangular pulses

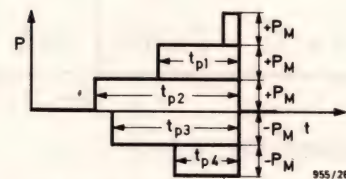


Fig.27 - Once-only rectangular composite pulse

SOAR for non-rectangular waveforms

Non-rectangular power pulses must be converted into power-equivalent rectangular pulses before SOAR boundaries can be constructed for them. For example, Figs.28a, 28b, and 28c show the variation of collector voltage and current with time for such a waveform. By multiplying together the instantaneous values of collector current and voltage, the collector power dissipation can be obtained. The equivalent rectangular pulse has the same energy (area) and the same maximum amplitude P_M , so that the equivalent pulse duration is given by:

$$t'_p = \frac{1}{P_M} \int_0^t P_{tot}(t) dt \dots (25)$$

For this example, integration gives:

$$t'_p = \frac{680}{6.3} = 108 \mu s.$$

For more complex waveforms, with several rise and fall phases or with sharply differing time-constants within such a phase, it is advisable to obtain a more accurate result by subdividing it into a number of equivalent pulses. Fig.29 shows an example of this procedure. The load limits for the rectangular pulse train now obtained (whether periodic or not) can then be determined by using the superimposition method previously discussed.

SOAR FOR $V_{CE} > V_{CEO \max}$

Operation at collector-emitter voltages greater than $V_{CEO \max}$ is possible only under restricted conditions. Safe operating areas published for transistors expected to be used in this region usually only cover certain special

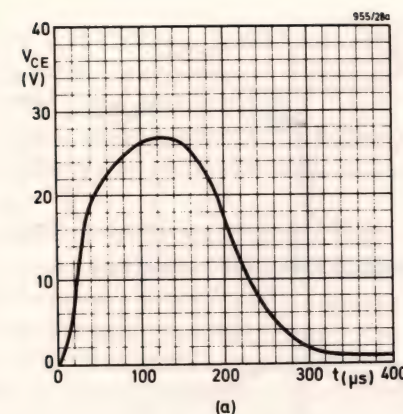


Fig.28 - Non-rectangular waveform:

(a) voltage characteristic

(b) current characteristic

(c) power dissipation and the equivalent rectangular pulse

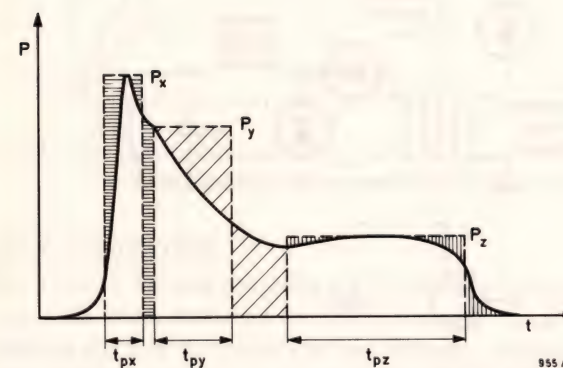
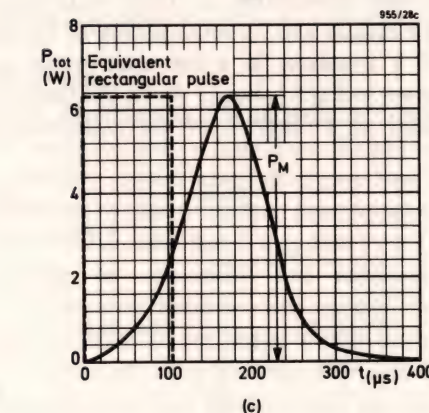
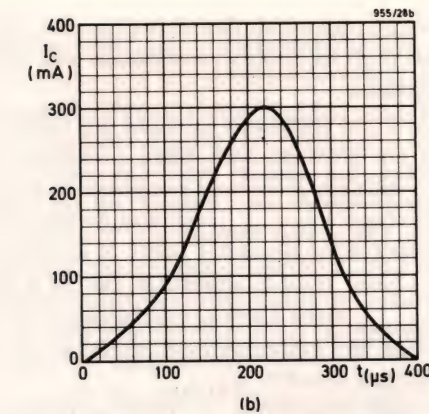


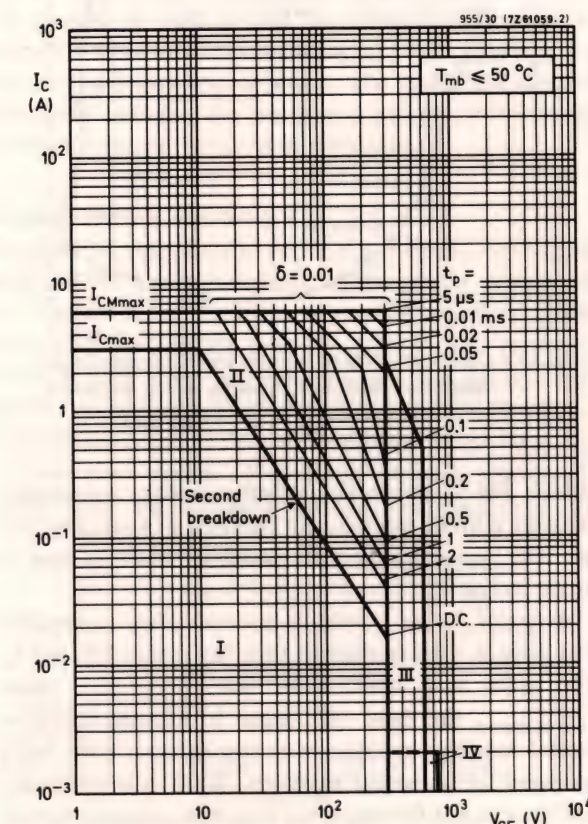
Fig.29 - A power variation of any shape can be subdivided into several equivalent rectangular pulses. The areas shown hatched in the same way above and below the curve are equal in size

cases, sections III and IV in Fig.30, for example. If the SOAR graph contains no safe operating area above $V_{CEO \max}$, the relevant transistor should only be operated up to boundary collector-emitter voltages dependent on the associated base conditions; that is:

up to voltage $V_{CBO \max}$ at $I_E = 0$,

up to voltage $V_{CEV \max}$ at a specified reverse voltage V_{BE} ,

up to voltage $V_{CER \max}$ at a specified resistance R_{BE} .

Fig.30 - Example of a SOAR with extensions for operation above $V_{CEO \max}$

The collector current which then flows may be only that which adjusts itself statically in accordance with the base control conditions.

The SOARs for transistors intended for high-voltage applications are provided with small extensions above $V_{CE0\max}$ which allow for brief excursions during turn-on. Turn-off above $V_{CE0\max}$ can also be allowed, but it is preferable for the operating point to remain below $V_{CE0\max}$: more reliable operation can be achieved below $V_{CE0\max}$ since thermal mechanisms are easier to control than the avalanche mechanisms which cause second breakdown above $V_{CE0\max}$.

The use and limitations of these extensions are illustrated by Figs.31 and 32 which represent the operating cycle of a transistor in a converter whose power circuit is shown in Fig.33. Fig.31 shows the base-emitter voltage plotted as a function of the collector-emitter

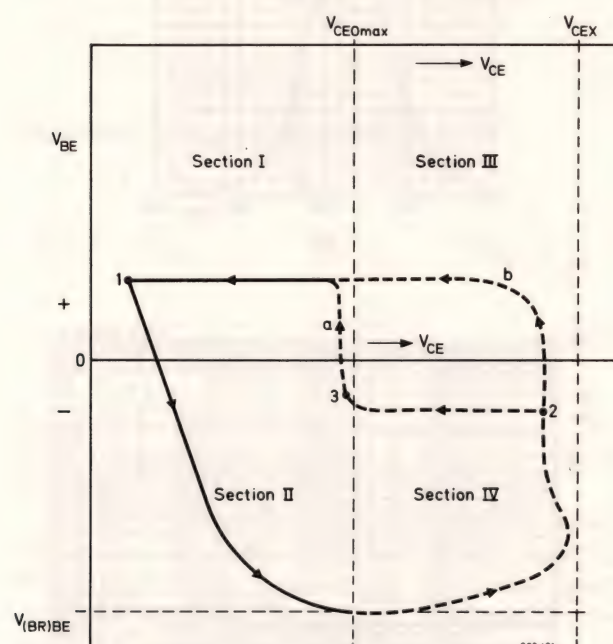


Fig.31 - Operating cycle of a power transistor used in an application such as a converter which includes a period when $V_{CE} > V_{CE0\max}$

voltage. Fig.32 shows the collector-emitter voltage and collector current plotted as a function of time; Figs.32a and 32b represent the two possible routes (a and b) shown in Fig.31.

At point 1, the transistor is conducting. A negative base drive is then applied to turn the device off, and I_C falls while V_{CE} rises. Now, when V_{CE} rises above $V_{CE0\max}$, the base will cease to exercise effective control over the emission of charge carriers, these being generated by avalanche injection. Thus, it is preferable that the current flowing when V_{CE} becomes greater than $V_{CE0\max}$ should be virtually zero although a small capacitive collector current (through the collector-

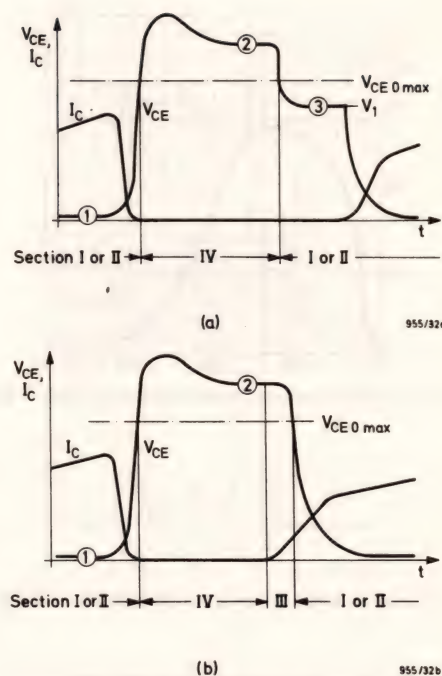


Fig.32 - Variation with time of the collector-emitter voltage and collector current of a d.c. converter:
(a) leaving area IV by cutting the transistor off;
(b) leaving area IV by switching the transistor on across area III

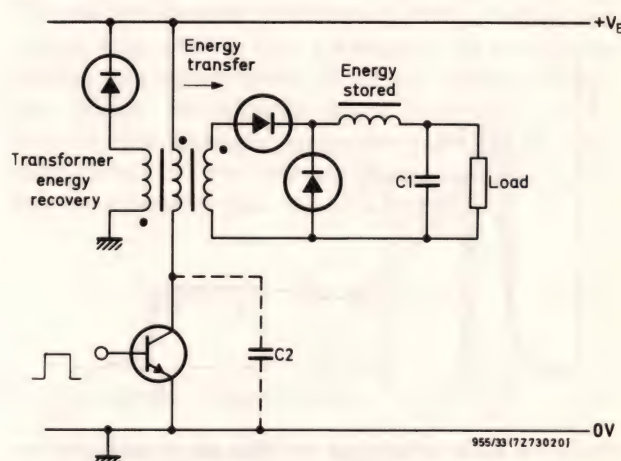


Fig.33 - Power circuit of a d.c.-to-d.c. converter (switched-mode power supply)

base and collector-heat-sink capacitances, for instance) is permitted. Section IV should be vacated within a few milliseconds by switching the transistor on by applying a positive voltage V_{BE} . Two routes are available, distinguished by a and b in Fig.31.

In case a, the collector-emitter voltage is first reduced to $V_{CE} < V_{CE0\max}$ and then the operating point passes through sections I and II, and the normal SOAR stipulations apply.

In case b, starting from point 2 ($V_{CE} > V_{CE0\max}$) section III is used. The variation in I_C and V_{CE} must be

so adjusted that the boundaries of section III in Fig.30 are not exceeded, and section I is reached within the time specified in the published data.

As indicated above, operation in both sections III and IV is restricted in terms of pulse time and base-emitter conditions.

When section III is used during turn-on, $V_{CE} > V_{CE0\max}$, and avalanche breakdown leading to second breakdown can only be avoided by a heavy injection of carriers into the base region. The base-emitter should be terminated by a base-emitter resistance R_{BE} of not more than 100Ω in case of, for instance, forward base drive by means of a current source. The value of collector-emitter voltage below which the device can safely be turned on, $V_{CE\text{ turn-on}}$, is dependent on both I_B and its rise time. The form of this dependence is similar to that shown in Fig.34, where V_{CE} is plotted against I_B with dI_B/dt as a parameter.

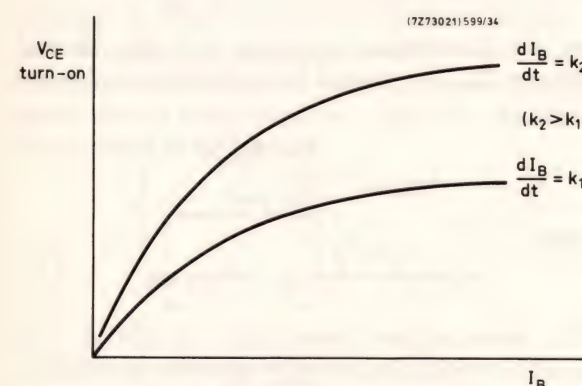


Fig.34 - The permissible value of V_{CE} during turn-on is a function of both the base drive current and its rate of rise

HEAT DISSIPATION

The limits to the safe operating area of power transistors have now been examined in detail and the means of adapting the safe operating area for different conditions explained. This section is not directly concerned with the safe operating area, but deals with the thermal operating conditions of power transistors.

All semiconductor failure mechanisms are temperature-dependent and so the lower the junction temperature, the higher the reliability of the circuit. Thus our data specifies a maximum junction temperature which should not be exceeded under the worst probable conditions. However, derating the operating temperature from $T_{j\max}$ is always desirable to improve the reliability still further. The junction temperature depends on both the power dissipated in the device and the thermal resistances (or impedances) associated with the device. Thus careful consideration of these thermal resistances (or impedances) allows the user to calculate the maximum power dissipation that will keep the junction temperature below a chosen value.

The formulae and diagrams given in this section can only be considered as a guide for determining the nature of a heatsink. This is because the thermal resistance of a heatsink depends on numerous parameters which cannot be predetermined. They include the position of the transistor on the heatsink, the extent to which air can flow unhindered, the ratio of the lengths of the sides of the heatsink, the screening effect of nearby components, and heating from these components. It is always advisable to check important temperatures in the finished equipment under the worst probable operating conditions. The more complex the heat dissipation conditions, the more important it becomes to carry out such checks.

Heat flow path

The heat generated in a semiconductor chip flows by various paths to the surroundings. Small-signal devices do not usually require heatsinking; the heat flows from the junction to the mounting base which is in close contact with the case. Heat is then lost by the case to the surroundings by convection and radiation (Fig.35a). Power transistors, however, are usually mounted on heatsinks because of the higher power dissipation they handle. Heat flows from the transistor case to the heatsink by way of contact pressure, and the heatsink loses heat to the surroundings by convection and radiation, or by conduction to cooling water (Fig.35b). Generally air cooling is used so that the ambient referred to in Fig.35 is usually the surrounding air. Note that if this is the air inside an equipment case, the additional thermal resistance between the inside and outside of the equipment case should be taken into account.

Contact thermal resistance $R_{th\ mb-h}$

The thermal resistance between the transistor mounting base and the heatsink depends on the quality and size of the contact areas, the type of any intermediate plates used, and the contact pressure. Care should be taken when drilling holes in heatsinks to avoid burring and distorting the metal, and both mating surfaces should be clean. Paint finishes of normal thickness, up to $50\mu\text{m}$ (as a protection against electrolytic voltage corrosion), barely affect the thermal resistance. Transistor case and

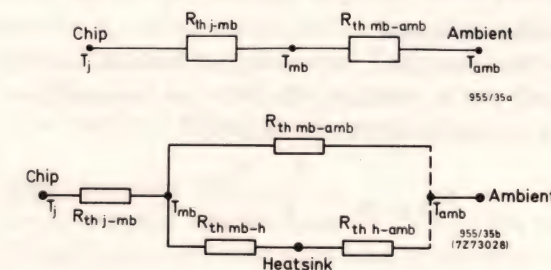


Fig.35 - Thermal resistances in the heat flow process:
(a) without a heatsink
(b) with a heatsink

heatsink surfaces can never be perfectly flat, and so contact will take place on several points only, with a small air-gap over the rest of the area. The use of a soft substance to fill this gap lowers the contact thermal resistance. Normally, the gap is filled with a heatsinking compound which remains fairly viscous at normal transistor operating temperatures and has a high thermal conductivity. The use of such a compound also prevents moisture from penetrating between the contact surfaces. Proprietary heatsinking compounds are available which consist of a silicone grease loaded with some electrically-insulating good thermally-conducting powder such as alumina. The contact thermal resistance $R_{th\ mb-h}$ is usually small with respect to $(R_{th\ j-mb} + R_{th\ h-amb})$ when cooling is by natural convection. However, the heatsink thermal resistance $R_{th\ h-amb}$ can be very small when either forced ventilation or water cooling are used, and thus a close thermal contact between the transistor case and heatsink becomes particularly important.

Thermal resistance calculations

Fig.35a shows that, when a heatsink is not used, the total thermal resistance between junction and ambient is given by:

$$R_{th\ j-amb} = R_{th\ h-mb} + R_{th\ mb-amb} \quad \dots (26)$$

However, power transistors are generally mounted on a heatsink since $R_{th\ j-amb}$ is not usually small enough to maintain temperatures within the chip below desired levels.

Fig.35b shows that, when a heatsink is used, the total thermal resistance is given by:

$$R_{th\ j-amb} = R_{th\ j-mb} + R_{th\ mb-h} + R_{th\ h-amb} \quad \dots (27)$$

Note that the direct heat loss from the transistor case to the surroundings through $R_{th\ mb-amb}$ is negligibly small.

The first stage in determining the size and nature of the required heatsink is to calculate the maximum heatsink thermal resistance $R_{th\ h-amb}$ that will maintain the junction temperature below the desired value.

Continuous operation

Under d.c. conditions, the maximum heatsink thermal resistance can be calculated directly from the maximum desired junction temperature. As in Eq.3,

$$R_{th\ j-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} \quad \dots (28)$$

and

$$R_{th\ j-mb} = \frac{T_j - T_{mb}}{P_{tot(av)}} \quad \dots (29)$$

Combining Eqs.27 and 28 gives:

$$R_{th\ h-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} - R_{th\ j-mb} - R_{th\ mb-h} \quad \dots (30)$$

and substituting Eq.29 into Eq.30 gives:

$$R_{th\ h-amb} = \frac{T_{mb} - T_{amb}}{P_{tot(av)}} - R_{th\ mb-h} \quad \dots (31)$$

The values of $R_{th\ j-mb}$ and $R_{th\ mb-h}$ are given in the published data. Thus, either Eq.30 or Eq.31 can be used to find the maximum heatsink thermal resistance.

Intermittent operation

The thermal equivalent circuits of Fig.35 are inappropriate to intermittent operation, and the thermal impedance $Z_{th\ j-mb}$ should be considered. Eq.7 states that:

$$P_{tot\ M} = \frac{T_j - T_{mb}}{Z_{th\ j-mb}},$$

and thus:

$$T_{mb} = T_j - P_{tot\ M} \cdot Z_{th\ j-mb} \quad \dots (32)$$

The mounting-base temperature has always been assumed to remain constant under intermittent operation. This assumption is known to be valid in practice provided that the pulse time is less than about one second. The mounting-base temperature does not change significantly under these conditions as indicated in Fig.36. This is because heatsinks have a high thermal capacity and thus a high thermal time-constant.

Thus Eq.31 is valid for intermittent operation, provided that the pulse time is less than one second. The value of T_{mb} can be calculated from Eq.32, and the

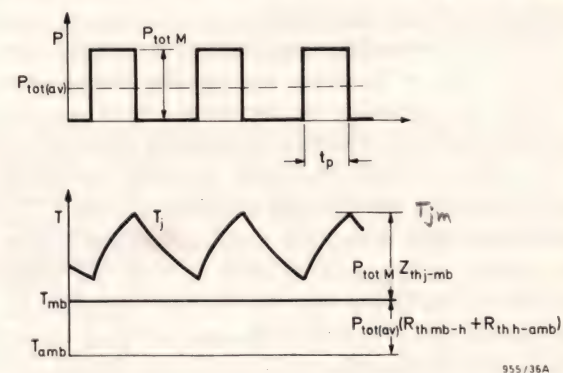


Fig.36 — Variation of junction and mounting-base temperatures when the pulse time is small compared with the thermal time-constant of the heatsink

heatsink thermal resistance can be obtained from Eq.31.

The thermal time-constant of a transistor is defined as that time at which the junction temperature has reached 70% of its final value after being subject to a constant power dissipation at a constant mounting-base temperature. For example, it is given in Fig.22 by the pulse duration at which:

$$Z_{th\ j-mb}(\delta = 0.01) = 0.7R_{th\ j-mb}.$$

Now, if the pulse duration t_p exceeds one second, the transistor is temporarily in thermal equilibrium since such a pulse duration is significantly greater than the thermal time-constant of most transistors. Consequently, for pulse times of more than one second, the temperature difference $T_j - T_{mb}$ reaches a stationary final value (Fig.37) and Eq.32 should be replaced by:

$$T_{mb} = T_j - P_{tot\ M} R_{th\ j-mb} \quad \dots (33)$$

In addition, it is no longer valid to assume that the mounting-base temperature is constant since the pulse time is also no longer small with respect to the thermal time-constant of the heatsink.

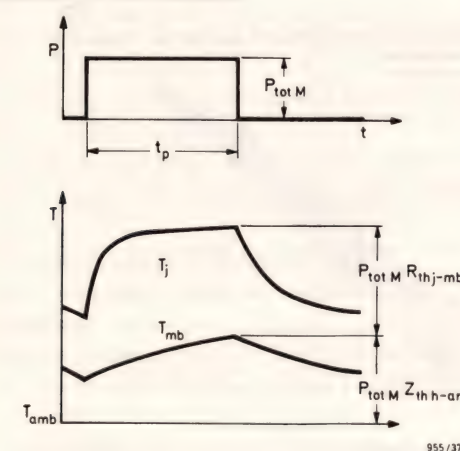


Fig.37 — Variation of the junction and mounting-base temperatures when the pulse time is not small compared with the thermal time-constant of the heatsink

Smaller heatsinks for intermittent operation

In many instances, the thermal capacity of a heatsink can be utilised to design a smaller heatsink for intermittent operation than would be necessary for the same level of continuous power dissipation. The average power dissipation in Eq.31 is replaced by the peak power dissipation to obtain the value of the thermal impedance between the heatsink and the surroundings:

$$Z_{th\ h-amb} = \frac{T_{mb} - T_{amb}}{P_{tot\ M}} - R_{th\ mb-h} \quad \dots (34)$$

The value of $Z_{th\ h-amb}$ will be less than the comparable thermal resistance and thus a smaller heatsink can be designed than that obtained using the too large value calculated from Eq.31.

HEATSINKS

Three varieties of heatsink are in common use: flat plates (including chassis), diecast finned heatsinks, and extruded finned heatsinks. The material normally used for heatsink construction is aluminium, although copper may be used with advantage for flat-sheet heatsinks. Small finned clips are sometimes used to improve the dissipation of low-power transistors.

Heatsink finish

Heatsink thermal resistance is a function of surface finish. A painted surface will have a greater emissivity than a bright unpainted one. The effect is most marked with flat-plate heatsinks, where about one-third of the heat is dissipated by radiation. The colour of the paint used is relatively unimportant, and the thermal resistance of a flat-plate heatsink painted gloss-white will be only about 3% higher than that of the same heatsink painted matt-black. With finned heatsinks, painting is less effective since heat radiated from most fins will fall on adjacent fins but it is still worthwhile. Both anodising and etching will decrease the thermal resistivity. Metallic-type paints, such as aluminium paint, have the lowest emissivities, although they are approximately ten times better than a bright aluminium metal finish.

Flat-plate heatsinks

The simplest type of heatsink is a flat metal plate to which the transistor is attached. Such heatsinks are used both in the form of separate plates and as the equipment chassis itself. The thermal resistance obtained depends on the thickness, area, and orientation of the plate, as well as on the finish and power dissipated. A plate mounted horizontally will have about twice the thermal resistance of a vertically-mounted plate. This is particularly important where the equipment chassis itself is used as the heatsink.

In Fig.38, the thermal resistance of a blackened heatsink is plotted against surface area (one side) with power dissipation as a parameter. The graph is accurate to within 25% for nearly square plates, where the ratio of the lengths of the sides is less than 1.25:1.

Finned heatsinks

Finned heatsinks may be made by stacking flat plates, although it is usually more economical to use ready-made diecast or extruded heatsinks. Since most commercially-available finned heatsinks are of reasonably optimum design, it is possible to compare them on the basis of the

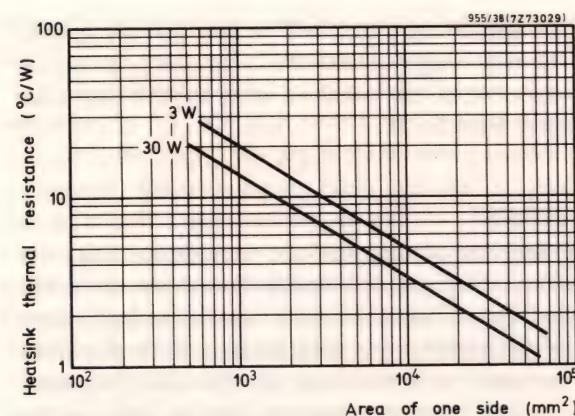


Fig.38 - Generalised heatsink characteristics: flat vertical black aluminium plates, 3mm thick, approximately square

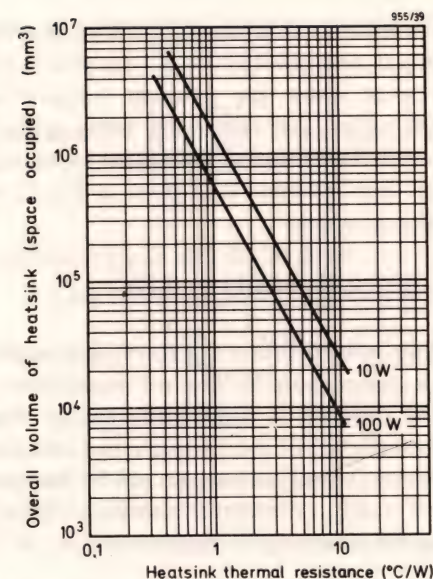


Fig.39 - Generalised heatsink characteristic: blackened aluminium finned heatsinks

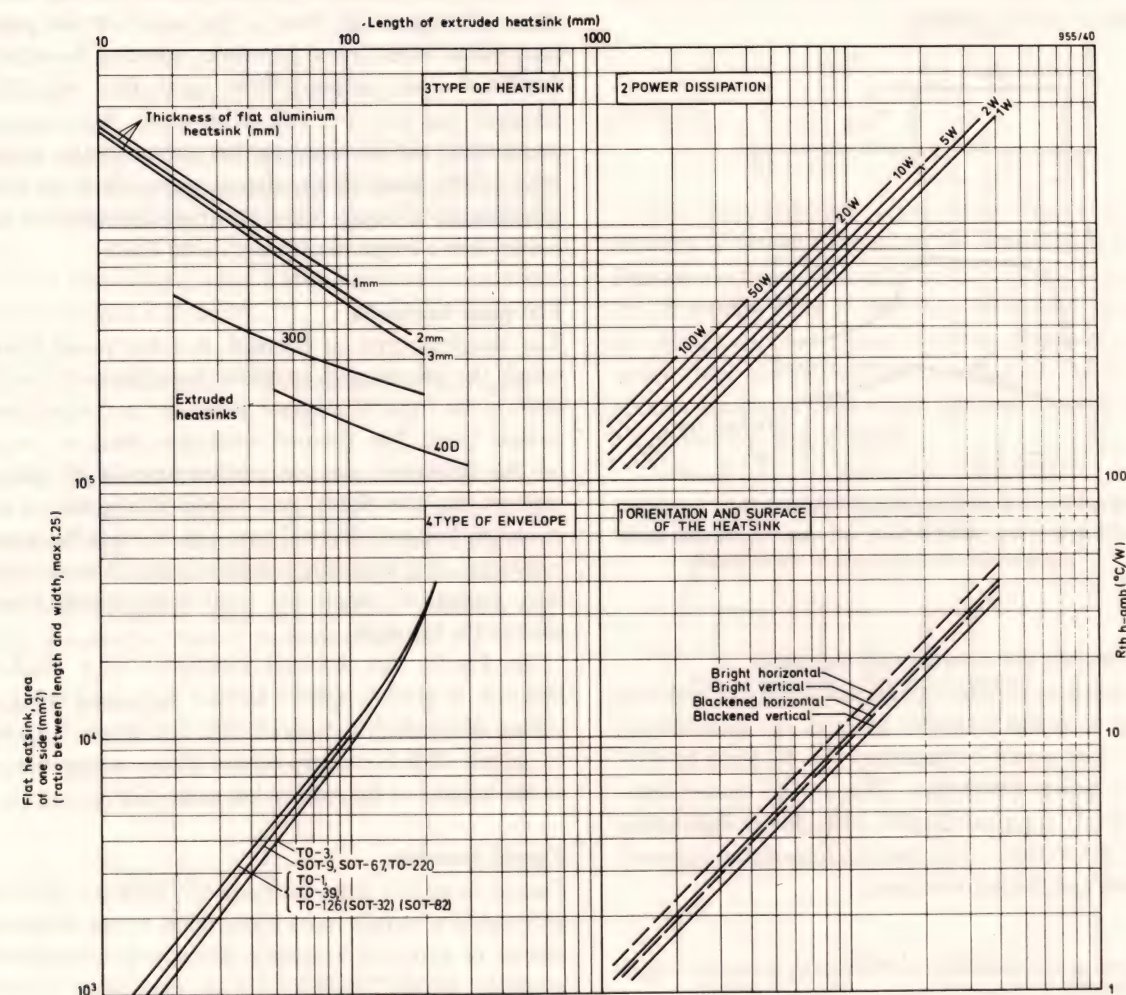


Fig.40 - Heatsink nomogram

overall volume which they occupy. This comparison is made in Fig.39 for heatsinks with their fins mounted vertically; again, the graph is accurate to 25%.

Heatsink dimensions

The maximum thermal resistance through which sufficient power can be dissipated without damaging the transistor can be calculated as discussed previously. This section explains how to arrive at a type and size of heatsink that gives a sufficiently low thermal resistance.

Natural air cooling

The required size of aluminium heatsinks - whether flat or extruded (finned) - can be derived from the nomogram in Fig.40. Like all heatsinks diagrams, the nomogram does not give exact values for $R_{th\ h-amb}$ as a function of the dimensions since the practical conditions always deviate to some extent from those under which the nomogram was drawn up. The actual values for the heatsink thermal resistance may differ by up to 10% from the nomogram values. Consequently, it is advisable to take temperature measurements in the finished equipment, particularly where the thermal conditions are critical.

The conditions to which the nomogram applies are as follows:

- natural air cooling (unimpeded natural convection with no build-up of heat);
- ambient temperature about 25°C, measured about 50mm below the lower edge of the heatsink (see Fig.41);
- atmospheric pressure about 10^5 N/m^2 ;
- single mounting (that is, not affected by nearby heatsinks);
- distance between the bottom of the heatsink and the base of a draught-free space about 100mm (see Fig.41);

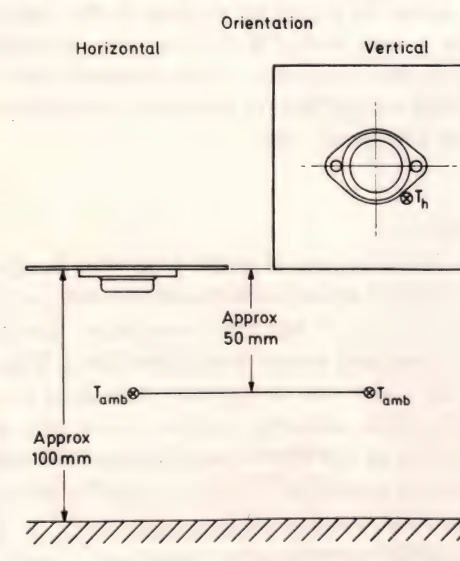


Fig.41 - Conditions applicable to nomogram in Fig.40

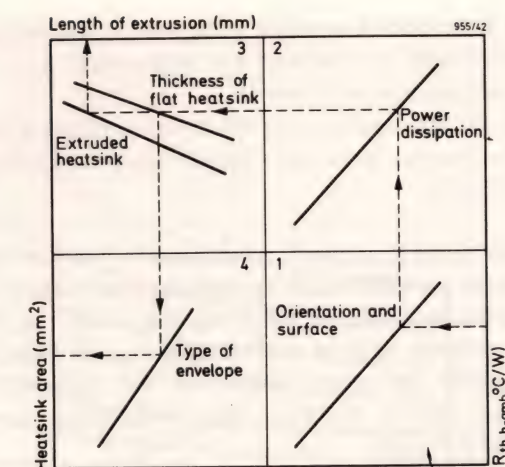


Fig.42 - Use of the heatsink nomogram (Fig.40)

- transistor mounted roughly in the centre of the heatsink (this is not so important for finned heatsinks because of the good thermal conduction).

The appropriately-sized heatsink is found as follows.

- 1) Enter the nomogram from the right-hand side of section 1 at the appropriate $R_{th\ h-amb}$ value (see Fig.42). Move horizontally to the left, until the appropriate curve for orientation and surface finish is reached.
- 2) Move vertically upwards to intersect the appropriate power dissipation curve in section 2.
- 3) Move horizontally to the left into section 3 for the desired thickness of a flat-plate heatsink, or the type of extrusion.
- 4) If an extruded heatsink is required, move vertically upwards to obtain its length (Figs.43a and 43b give the outlines of the extrusions).

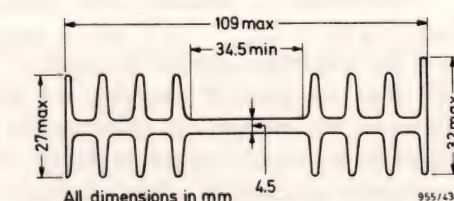


Fig.43a - Outline of extrusion 30D

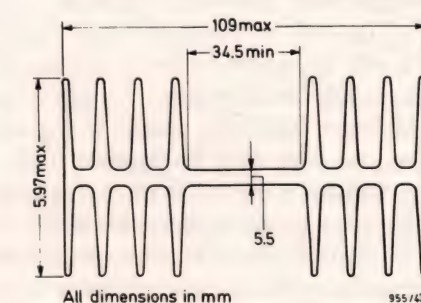


Fig.43b - Outline of extrusion 40D

- 5) If a flat-plate heatsink is to be used, move vertically downwards to intersect the appropriate curve for envelope type in section 4.
- 6) Move horizontally to the left to obtain heatsink area.
- 7) The heatsink dimensions should not exceed the ratio of 1.25:1.

The curves in section 2 take account of the non-linear nature of the relationship between the temperature drop across the heatsink and the power dissipation loss. Thus, at a constant value of the heatsink thermal resistance, the greater the power dissipation, the smaller is the required size of heatsink. This is illustrated by the following example.

Example 9

An extruded heatsink mounted vertically and with a painted surface is required to have a maximum thermal resistance of $R_{th\ h-amb} = 2.6^\circ\text{C/W}$ at the following powers:

- a) $P_{tot(av)} = 5\text{W}$, b) $P_{tot(av)} = 50\text{W}$.

Enter the nomogram at the appropriate value of the thermal resistance in section 1, and via either the 50W or 5W line in section 2, the appropriate lengths of the extruded heatsink 30D are found to be:

- a) length = 110mm and b) length = 44mm.

Case b) requires a shorter length since the temperature difference is ten times greater than in case a).

As the ambient temperature increases beyond 25°C , so does the temperature of the heatsink and thus the thermal resistance (at constant power) decreases owing to the increasing role of radiation in the heat removal process. Consequently, a heatsink with dimensions derived from Fig.40 at $T_{amb} > 25^\circ\text{C}$ will be more than adequate. If the maximum ambient temperature is less than 25°C , then the thermal resistance will increase slightly. However, any increase will lie within the limits of accuracy of the nomogram and within the limits set by other uncertainties associated with heatsink calculations.

For heatsinks with relatively small areas, a considerable part of the heat is dissipated from the transistor case. This is why the curves in section 4 tend to flatten out with decreasing heatsink area. The area of extruded heatsinks is always large with respect to the surface of the transistor case, even when the length is small.

If several transistors are mounted on a common heatsink, each transistor should be associated with a particular section of the heatsink (either an area or length according to type) whose maximum thermal resistance is calculated from Eqs.30 or 31; that is, without taking the heat

produced by nearby transistors into account. From the sum of these areas or lengths, the size of the common heatsink can then be obtained. If a flat heatsink is used, the transistors are best arranged as shown in Fig.44. The maximum mounting-base temperatures of transistors in such a grouping should always be checked once the equipment has been constructed.

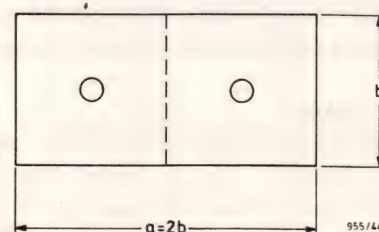


Fig.44 — Arrangement of two equally loaded transistors mounted on a common heatsink

Forced air cooling

If the thermal resistance needs to be much less than 1°C/W , or the heatsink not too large, forced air cooling by means of fans can be provided. Apart from the size of the heatsink, the thermal resistance now only depends on the speed of the cooling air. Provided that the cooling air flows parallel to the fins and with sufficient speed ($v > 0.5\text{m/s}$), the thermal resistance hardly depends on the power dissipation and the orientation of the heatsink. Note that turbulence in the air current can result in practical values deviating from theoretical values.

Fig.45 shows the form in which the thermal resistances for forced air cooling are given in the case of extruded heatsinks and the reduction in thermal resistance or length of heatsink which may be obtained with forced air cooling.

The effect of forced air cooling in the case of flat heatsinks is seen from Fig.46. Here, too, the dissipated power and the orientation of the heatsink have only a slight effect on the thermal resistance, provided that the air flow is sufficiently fast.

SUMMARY

The safe operating area of power transistors is a graph of collector current against collector-emitter voltage plotted on a log-log grid. It has four boundaries: the current, voltage, power, and second breakdown limits. This graph enables the device user to operate a transistor to its full capabilities while ensuring that the device will operate reliably. Each of the four boundaries should be regarded as an absolute maximum; driving a transistor into second breakdown will result in sudden destruction, or at least damage, while exceeding the current and power limits can result in reduced life.

Fig.45 — Thermal resistance of a finned heatsink (extrusion type 40D) as a function of length with natural and forced air cooling

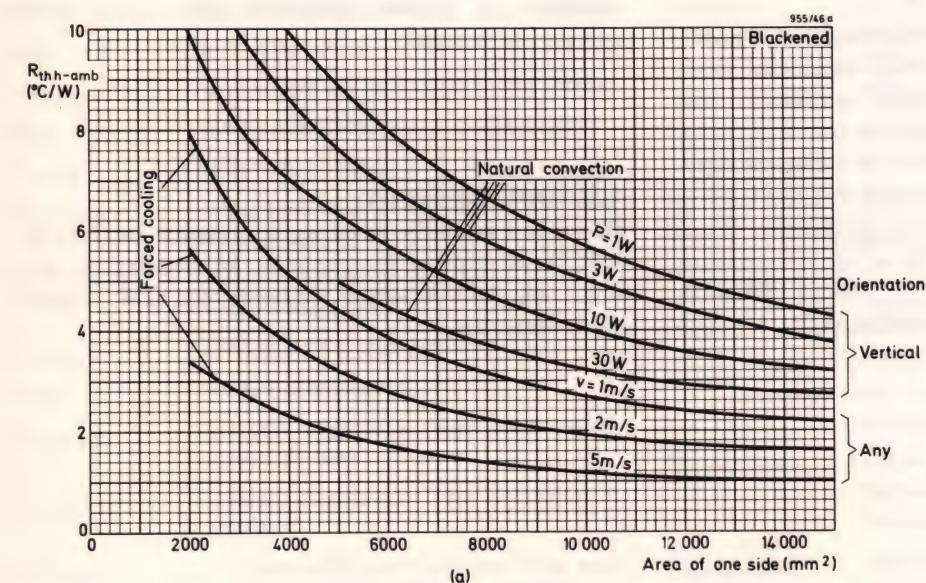
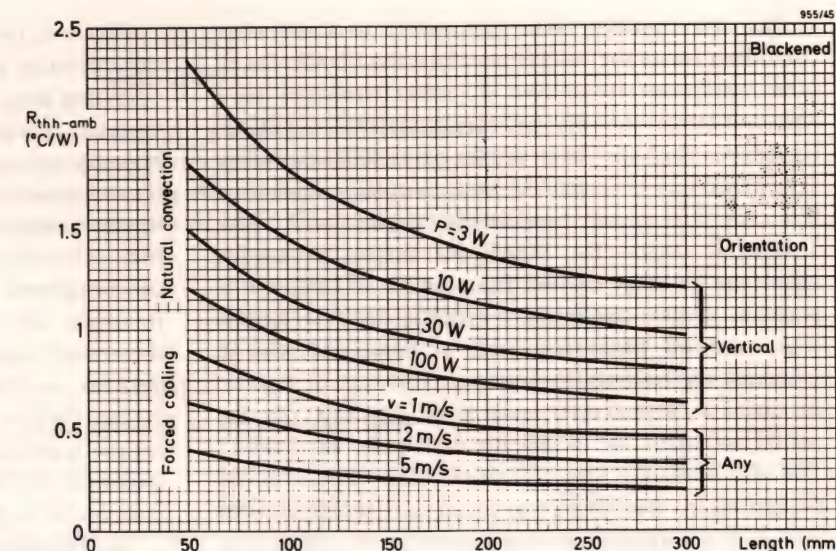
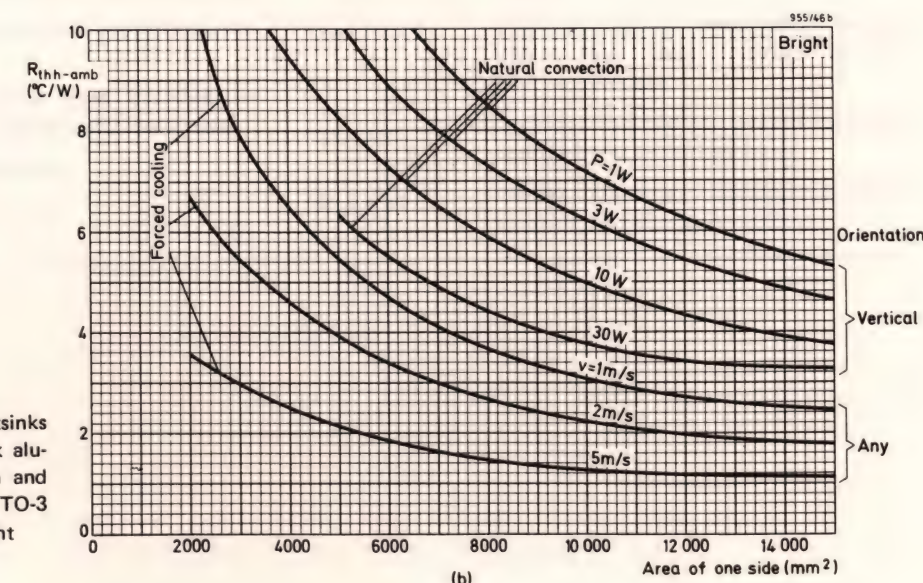


Fig.46 — Thermal resistances of heatsinks (2mm thick copper or 3mm thick aluminium) under natural convection and forced cooling conditions, with a TO-3 envelope: (a) blackened (b) bright



The safe operating area appropriate to steady-state conditions forms the basis from which the SOARs for all other conditions are derived. A power transistor has a definite thermal capacity, and consequently all the SOAR boundaries that are either wholly or partially thermally determined can be extended for intermittent operation; these are the second breakdown, current, and power dissipation limits. The SOAR for simple rectangular pulses can be easily derived from the d.c. SOAR, but, in practice, power transistors frequently have to handle more complex waveforms, such as those occurring in switching applications, for instance. This type of signal is simulated by several rectangular pulses having a common period and then the SOAR for each pulse is obtained. The safe operating area of non-periodic waveforms can be derived by assuming a very small duty factor, and the SOAR of non-rectangular waveforms can be constructed by converting the waveform into one or more power-equivalent rectangular pulses.

The voltage limit to the safe operating area is usually $V_{CEO\ max}$, the voltage below which avalanche breakdown cannot occur. Great care should be taken to avoid second breakdown when operating above $V_{CEO\ max}$ since second breakdown is triggered by avalanche injection which is more difficult to control than the thermal mechanisms which cause second breakdown below $V_{CEO\ max}$. However, the SOARs of some transistors include extensions above $V_{CEO\ max}$ which allow for brief excursions under restricted conditions.

However, not only should care be taken to ensure that the operating point of a device remains within its safe operating area, but also attention should be given to the thermal resistances associated with the device. The majority of power transistors require heatsinking, and once the maximum thermal resistance that will maintain the device's junction temperature below its rating has been calculated, a heatsink of appropriate type and size can be chosen. The practical conditions under which a transistor will be operated are likely to differ from the theoretical considerations used to determine the required heatsink, and thus temperatures should always be checked in the finished equipment. Finally, some applications require a small heatsink, or one with a very low thermal resistance, in which case forced air cooling by means of fans should be provided.

In Appendix 4 a flow chart is shown which summarises the procedure for checking the suitability of a particular transistor for a given application, and arriving at an appropriate heatsink.

ACKNOWLEDGEMENT

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APPENDIX 1

Definitions

The various parameters for transistors and associated components referred to in this article have been assigned standard abbreviations. The abbreviations used are based upon the recommendations of IEC 148 and are listed in Table 2.

TABLE 2
List of Letter Symbols in Alphabetical Order

Letter symbol	Definition	Letter symbol	Definition
δ	pulse duty factor	T_{mb}	mounting-base temperature
I_C, I_B	d.c. (or average) current	$T_{mb\ K}$	the value of T_{mb} above which the maximum power dissipation must be reduced to keep the device within the safe operating area
I_{CM}	peak value of I_C	ΔT_{j-mb}	temperature difference (junction to mounting base)
$M_{SB(V)}, M_{SB(I)}$	voltage and current multiplying factors	t_p	pulse duration
P_{tot}	total power dissipation in the device	T	pulse period
$P_{tot\ M}$	peak value of P_{tot}	V_{CE}, V_{BE}	d.c. (or average) voltage
$P_{tot\ max}$	maximum value of P_{tot} at $T_{mb} > T_{mb\ K}$	V_{CES}	collector-emitter voltage with $V_{BE} = 0$
$P_{tot\ max\ K}$	maximum value of P_{tot} at $T_{mb} < T_{mb\ K}$	V_{CEO}, V_{CBO}	collector-emitter or collector-base voltage with the third terminal open-circuited
$P_{tot(av)}$	average power dissipation	V_{CER}, V_{CEV}	collector-emitter voltage with a specified resistance or reverse voltage between base and emitter
R_{BE}	base-emitter resistance	$V_{(BR)\ CEO}$	collector-emitter breakdown voltage with $I_B = 0$
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$V_{(BR)\ CEV}$	collector-emitter breakdown voltage with a peak reverse voltage between base and emitter
$R_{th\ j-amb}$	thermal resistance from junction to ambient	$Z_{th\ j-mb}$	transient thermal impedance between junction and mounting base
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink (contact thermal resistance)	$Z_{th\ h-amb}$	transient thermal impedance between heatsink and the surroundings
$R_{th\ mb-amb}$	thermal resistance from mounting base to ambient		
$R_{th\ h-amb}$	thermal resistance from heatsink to ambient (heatsink thermal resistance)		
T_j	junction temperature		
T_{amb}	ambient temperature		

APPENDIX 2

Second Breakdown

It can be shown that, if there is no base or emitter resistance, the input resistance of a transistor will become negative if the temperature difference ΔT_{j-mb} between its junction and the bottom of the chip (mounting base) exceeds 16°C . This is explained in Appendix 3. Consider a power transistor model consisting of a number of parallel-connected elemental transistors, none of which has base or emitter resistance (Fig.47). Assume that the elements are otherwise isolated both electrically and thermally, so that the temperature of any one element is independent of the temperature of the others. If the

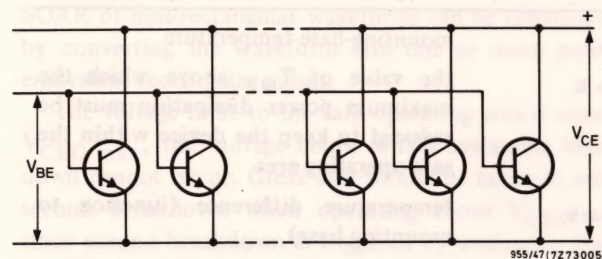


Fig.47 — A complete power transistor may be considered to be composed of a large number of paralleled elements

model is provided with a constant V_{CE} and driven so that I_C increases steadily, current increase will be accompanied by an increase in ΔT_{j-mb} because of the power dissipation. The individual transistors comprising the model do not have identical electrical characteristics nor are they in identical thermal environments, so that one of them will attain the critical value of ΔT_{j-mb} first. Its input resistance will go negative, drawing all the base current. The temperature of this transistor will then increase rapidly until eventually the diffusion of the emitter and collector regions will penetrate further, culminating in a short-circuit between emitter and collector, as shown in Fig.48.

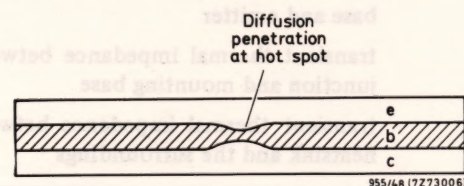


Fig.48 — Damage due to second breakdown

There is, in practice, always a certain amount of thermal coupling between the various parts of a power transistor. Also, the edges of a chip will be more effectively cooled than the middle. Therefore under conditions of uniform current density, the temperature in the middle of a chip will rise more quickly than at the edges (Fig.49), and the critical value of ΔT_{j-mb} will be reached first in the middle.

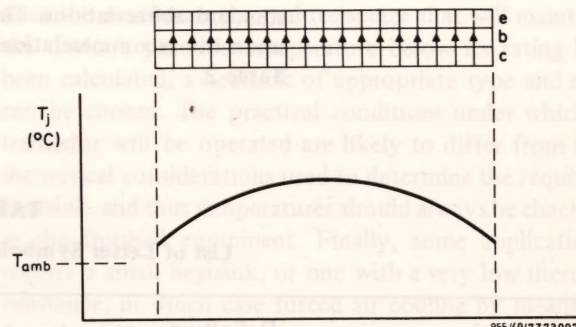


Fig.49 — Because of better heat dissipation, the edges of a transistor chip are cooler than the middle when the current density is uniform over the chip area

The second breakdown mechanism can be considered with respect to the four I_C/V_{CE} points in Fig.50. Point A represents operation at high collector current and low collector-emitter voltage ($V_{CE} < V_{CE0\max}$) with $I_B > 0$. The current flow in a transistor under these conditions is shown in Fig.51. Since the base region must have some bulk resistivity, the current flow through the base produces a progressive voltage drop towards the centre of the emitter. As a result, the transistor is more heavily biased towards the edge of the emitter and thus the current tends to flow more heavily at the edges of the emitter.

Point B represents high collector current combined

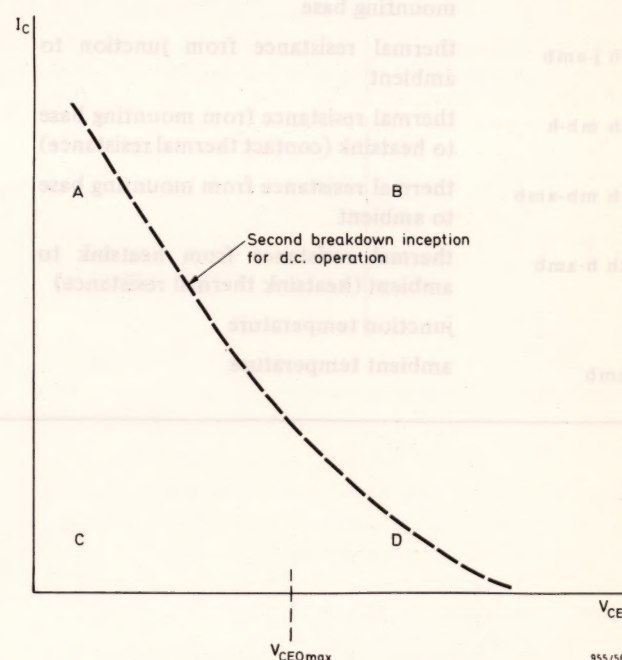


Fig.50 — The locus of second breakdown inception under d.c. conditions

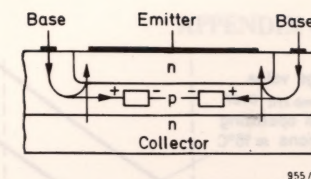


Fig.51 — Representation of the current distribution in a transistor chip when $I_B > 0$ ($V_{CE} < V_{CE0\max}$); applicable to low frequencies only

with high collector-emitter voltage, and the power is such that damage to the transistor is inevitable.

Point C represents low collector current with low collector-emitter voltage, and as the transistor is operating well within its ratings, safe operation is assured.

Point D represents operation at low collector current and high collector-emitter voltage ($V_{CE} > V_{CE0\max}$) with $I_B < 0$ (Fig.52). Again, the base current will cause a

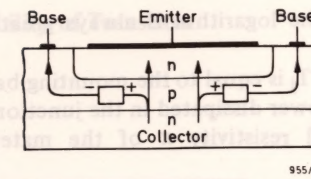


Fig.52 — Representation of the current distribution in a transistor chip when $I_B < 0$ ($V_{CE} > V_{CE0\max}$); applicable to low frequencies only

voltage drop across the emitter, which in this instance causes a concentration of current flow into the centre of the emitter.

Thus, base current causes an uneven distribution of current over the emitter which results in current concentration and the danger of second breakdown occurring at lower power dissipation levels than would be expected if the current was evenly distributed over the emitter.

APPENDIX 3

The Influence of ΔT_{j-mb} on Transistor Input Resistance

Consider the case of an elemental transistor having only length (Fig.53). The lengths of the emitter, base, and collector regions are Δe , Δb , and Δc respectively. The current density through the device may be written:

$$J = J_0 (e^{qV_{BE}/kT_j} - 1) \quad \dots (35)$$

where J_0 is the saturation current, meaning, in this case, the current flowing when $V_{BE} < 0$. When $V_{BE} > 0.1\text{V}$, the (-1) component can be neglected.

It follows from Eq.35 that J increases with V_{BE} and decreases with increasing temperature. Now J_0 is also temperature-dependent, being given by:

$$J_0 = 1.5 \times 10^{45} \times q \frac{D_n}{\Delta b} T_j^\beta \cdot e^{-qV_g/kT_j} \int_0^{\Delta b} p_p dx \quad \dots (36)$$

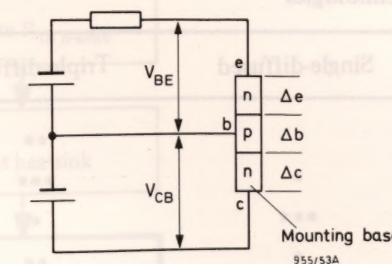


Fig.53 — Elemental transistor

where D_n is the diffusion constant for the n-type region, p_p is the hole density in the p-type region, and β is a constant whose value lies between 2 and 3.

Part of Eq.36 is the free electron density of the intrinsic material n_i such that:

$$n_i^2 = 1.5 \times 10^{45} \times T_j^\beta \cdot e^{-qV_g/kT_j} \quad \dots (37)$$

The temperature-dependence of D_n may be neglected, so, collecting together the temperature-dependent components:

$$J = CT_j^\beta e^{q(V_{BE}-V_g)/kT_j} \quad \dots (38)$$

where:

$$C = 1.5 \times 10^{45} \times q \frac{D_n}{\Delta b} \int_0^{\Delta b} p_p dx$$

Eq.38 may be rewritten to give V_{BE} :

$$V_{BE} = V_g - \frac{kT_j}{q} \log_e \frac{CT_j^\beta}{J} \quad \dots (39)$$

It may be seen from Eq.39 that whereas V_{BE} increases slowly with increasing J , it decreases quickly as T_j increases, since at normally-encountered values of J , the

numerator of the logarithm is always greater than the denominator.

The value of T_j is equal to the mounting-base temperature plus the power dissipated in the junction multiplied by the thermal resistivity κ of the material of the transistor:

$$T_j = T_{mb} + J V_{CE} \Delta \epsilon \kappa, \quad \dots (40a)$$

or:

$$T_j = T_{mb} + AJ, \quad \dots (40b)$$

where $A = V_{CE} \Delta \epsilon \kappa$, a constant.

Substituting this expression for T_j into Eq.39 yields:

$$V_{BE} = V_g - \frac{k(T_{mb} + AJ)}{q} \log_e \frac{CA(T_{mb} + AJ)^\beta}{J} \quad \dots (41)$$

If the value of V_{BE} from this equation is plotted against J , as in Fig.54, there is a maximum value for V_{BE} .

Now, from Eq.40b, it follows that $\Delta T_{j-mb} = AJ$, and is the temperature increase due to the device dissipation.

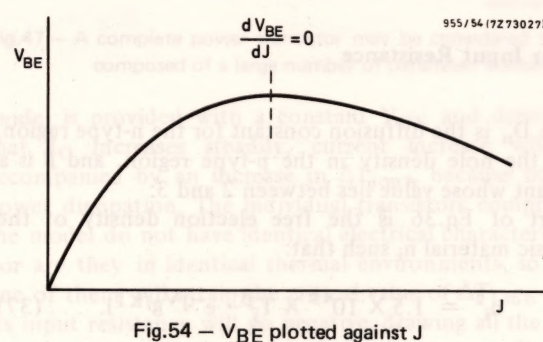


Fig.54 - V_{BE} plotted against J

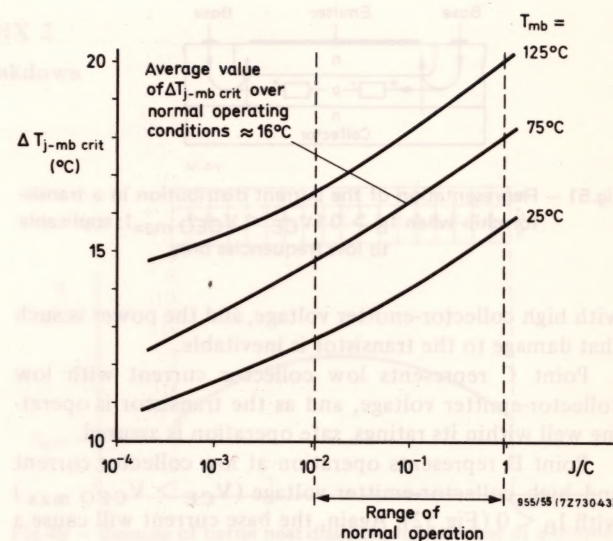


Fig.55 - ΔT_{j-mb} crit plotted against J/C

It can be shown that, when $dV_{BE}/dJ = 0$:

$$\Delta T_{j-mb} = \frac{T_{mb}}{\beta - 1 + \ln(CT_j^\beta/J)} = \Delta T_{j-mb} \text{ crit}, \quad \dots (42)$$

the temperature at which the transistor input resistance goes negative, and runaway occurs. It can be seen that ΔT_{j-mb} crit is proportional to T_{mb} , and increases as C/J reduces.

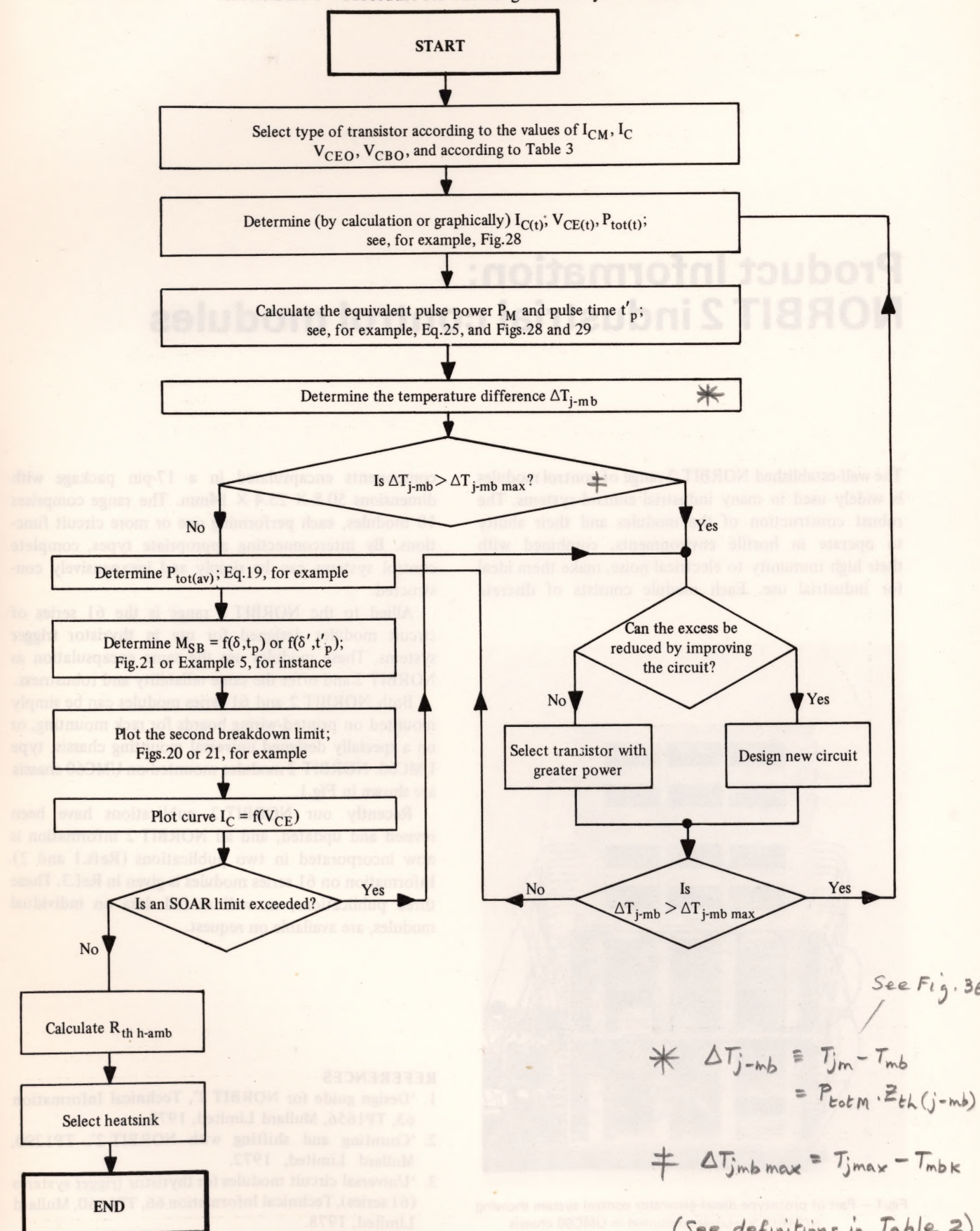
All the information required to calculate ΔT_{j-mb} crit is available, and Fig.55 shows some values plotted for silicon. It can be seen that, over the normal operation range of silicon devices, the average value of ΔT_{j-mb} crit is approximately 16°C .

TABLE 3

Properties of Various Transistor Technologies

Technology	Planar	Epitaxial-base	Single-diffused	Triple-diffused
Switching speed	***	*		**
Breakdown voltage	**	**	*	***
SOAR		**	***	*
Saturation voltage	***	**	*	**

APPENDIX 4 - Procedure for Checking Suitability of Transistor



Product Information: NORBIT 2 industrial control modules

The well-established NORBIT 2 range of control modules is widely used in many industrial control systems. The robust construction of the modules and their ability to operate in hostile environments, combined with their high immunity to electrical noise, make them ideal for industrial use. Each module consists of discrete

components encapsulated in a 17-pin package with dimensions 50.8 X 25.4 X 14mm. The range comprises 10 modules, each performing one or more circuit functions. By interconnecting appropriate types, complete control systems can be simply and inexpensively constructed.

Allied to the NORBIT 2 range is the 61 series of circuit modules designed for use in thyristor trigger systems. These modules use the same encapsulation as NORBIT 2 and offer the same reliability and robustness.

Both NORBIT 2 and 61 series modules can be simply mounted on printed-wiring boards for rack mounting, or on a specially designed universal mounting chassis, type UMC60. NORBIT 2 modules mounted on UMC60 chassis are shown in Fig.1.

Recently our NORBIT 2 publications have been revised and updated, and all NORBIT 2 information is now incorporated in two publications (Refs.1 and 2). Information on 61 series modules is given in Ref.3. These three publications, as well as full data on individual modules, are available on request.

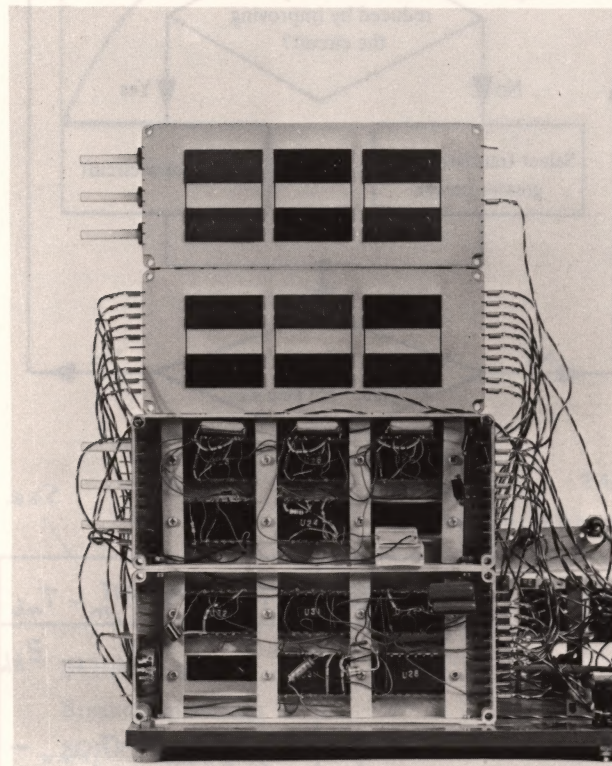


Fig.1 — Part of prototype diesel-generator control system showing NORBIT 2 modules mounted in UMC60 chassis

REFERENCES

1. 'Design guide for NORBIT 2', Technical Information 63, TP1656, Mullard Limited, 1978.
2. 'Counting and shifting with NORBIT 2', TP1290, Mullard Limited, 1972.
3. 'Universal circuit modules for thyristor trigger systems (61 series), Technical Information 66, TP1660, Mullard Limited, 1978.